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PBX SYSTEMS
51A CUSTOMER PREMISES SYSTEM
CENTREX DATA RECEIVER
AND TRANSMITTER CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 It is the purpose of the data receiver and transmitter circuit to:

(a) Recognize mark and space signals in the received line signal based upon a predetermined method of signaling.

(b) Accept mark and space signals at a rate of 1400 bits per second (BPS).

(c) Provide means for transmitting the contents of the shift register in synchronization with the received data.

(d) Provide means to recognize the operation of a key and identify the key.

(e) Place a request on the data loop to transmit the key identity stored in the local shift register.

(f) Provide means for recognizing the start and determining the end of a transmitted data word.

(g) Provide means for determining proper parity of the received word and transmitting the result of the parity match to the central office by means of a specially transmitted all-seems-well (ASW) bit.

(h) Signal the lamp control circuit that a lamp order or interrogate order has been received.

(i) Provide means for detecting the absence of signals on the incoming line.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The centrex data receiver expects to see a frequency-shift type line signal that will carry the binary intelligence in terms of 700- or 2100-Hz sinusoidal waveforms. The data receiver determines the presence of a mark or a space based upon an amplitude-sampling principle. The data receiver is kept in synchronization with the fundamental 1400-Hz bit rate by a pair of free-running local oscillators, 700- and 2100-Hz circuits.

2.02 In an idle mode, the circuit expects to find a steady 700-Hz tone on the line. The data receiver and transmitter will apply a similar 700-Hz tone to the return line. In this idling mode, the data receiver is constantly sampling the line for a mark signal which indicates start of transmission. The recognition of such an initial mark changes the data circuit from an idle to an active data-receiving mode. The absence of signals or tone on the incoming line for a period of more than 40 ms will cause the local oscillator to

stop, thus removing the signals from the outgoing line.

2.03 The data receiver and transmitter determine the end of transmission by counting the bits received. The proper bit count will automatically return both the receiver and transmitter to an idle mode.

2.04 The recognized mark and space signals are converted into 0s and 1s and inserted into a shift register. The shift register stores the received bits, converts the previously stored information from parallel form into a series combination of mark and space signals, and transmits them back to the central office.

2.05 The circuit responds to the operation of a number of keys and translates the operated key into a preassigned 5-digit binary number. In the busy state, the circuit delays the response of the operated keys until the circuit is in an idle state.

2.06 The circuit also determines whether the word just received in the shift register is to change the state of some lamp activated by the connecting circuit or to investigate general performance of the data receiver and transmitter. Such diagnostic activities are recognized by a diagnostic code.

2.07 Synchronization between receiver and received line signals is insured by means of intense coupling between line amplifier and local oscillators. Line-to-oscillator coupling compensates for phase distortion and envelope delay, and the internal circuitry insures mutual frequency-tracking and proper phase relationship between the free-running oscillators.

SECTION II - DETAILED DESCRIPTION

1. DATA RECEIVER - FS 1

1.01 The data receiver should be connected to a regular pair of exchange cables. An incoming line is assumed to be an ordinary speech transmission path. The line amplifier (circuit LA) provides for the necessary gain, which approximates 30 dB, and delivers the amplified signal on terminals 2 and 4. The amplified line signals appear on these two terminals 180 degrees out of phase. The line amplifier also supplies its output terminal 1 with the amplified line signal which is connected to the local oscillators to maintain proper phase relationship between the local 700-Hz oscillator and the line signal. In this manner, bit synchronization is maintained. The received line signal is expected to contain either a 700- or 2100-Hz signal. If a 2100-Hz signal is present, it is converted to a 700-Hz signal on line amplifier terminal 1 by means of the sampling signals connected to the line amplifier terminals 5 and 6. The absence of a signal on terminal 2 or 4 of the LA circuit will cause the NS flip-flop to remain in the set or reset state. This state will place a high condition on either terminal 20 or 22 of the AT circuit. The absence of a low condition on one of its inputs for a time greater than 40 ms will cause output terminal 11 of the AT circuit to go low. This low condition applied to terminals 3 and 5 of the OSC circuit will stop the oscillators and remove the idling tone from the outgoing line. Therefore, the absence of signals on the incoming line will remove the signals applied to the outgoing line.

1.02 The data receiver contains two free-running oscillators. The receiver also contains circuits which generate synchronizing pulses and circuits which provide the necessary impedance and tone level gain. The oscillator buffer circuit (OSC) delivers the two sinusoidal tones on its output terminals 1 and 25. These terminals are connected to leads L and H. The two tones are present on these two leads as a continuous waveform, and they serve as the main source for the transmitting tone signals. The buffer circuit provides for two sampling pulses, one-third of a bit slot wide, which appear on terminals 10 and 19 and occur at the center of each bit slot. These pulses sample the signal present on the line and, by means of the line-signal sampler, determine if the line signal contains a mark or a space. When a mark signal has been found, an output signal appears on terminal 22 of the line-signal sampler. This negative pulse will set flip-flop MS. The same output pulse appears inverted on terminals 10 and 20 of the line-signal sampler. This positive pulse is connected to circuit ST. The first positive pulse found by the sampling pulses determines the start of transmission. Marks are detected only during the middle one-third of the bit slot. The MS flip-flop remains set until the next 0-crossing and is then reset. A space is not actually detected, but is the absence of marks.

1.03 Synchronizing pulses are generated by the 0-crossing (zero-crossing) sync generator (SYNC). This circuit is driven from the local 700-Hz oscillator and provides timing pulses which occur at the 0-crossing time of the local 700-Hz oscillator. The time when the oscillator output signal passes through local circuit ground with a positive or negative slope is a 0-crossing (zero-crossing). Each time such a crossing occurs, a negative pulse appears on terminal 2 of the synchronizing generator. The leading edge of this negative pulse coincides with the 0-crossing time; pulse width is approximately 40 USEC. Terminal 27 of the same circuit is a local reset pulse and is also a negative pulse. This pulse occurs immediately after the synchronizing pulse has disappeared and is approximately 80 USEC wide. These two synchronizing

pulses provide for the internal sequencing and sampling of data which has been recognized by the circuit. The same circuit provides square-wave pulses on its output terminals 6 and 4. The pulse present on terminal 4 is positive during the time the 700-Hz oscillator waveform is positive with respect to circuit ground. Similarly, terminal 6 has a negative pulse during the time that the 700-Hz oscillator is negative with respect to local circuit ground.

1.04 One function of the 0-crossing pulses is to maintain proper phase relationship between the two local oscillators. This synchronizing pulse corrects for any phase discrepancy once every cycle of the 700-Hz oscillator. This pulse is generated by the 0-crossing sync generator and gate INV0. This loop causes a 40-USEC pause of both local oscillators each time the 700-Hz signal passes through zero with a positive slope.

1.05 The state of flip-flop SS determines whether the data receiver is active or idle. If the line signal changes from a steady idling 700-Hz tone to an initial mark signal, the data receiver changes from an idle to an active transmitting mode. The end of a transmitted word is then determined by the bit counter shown on FS 2. The data receiver is idle when flip-flop SS is reset.

1.06 When an initial mark is detected, a negative pulse present on terminal 22 of the line-signal sampler will set flip-flop MS. Simultaneously, the positive pulse appearing on terminal 10 of the line-signal sampler will be present on terminal 19 of circuit ST. When such a pulse is present on that terminal at a time when terminal 20 of the same circuit is high, a negative pulse appears on output terminal 21 of circuit ST. This negative pulse will reset local parity counter circuit PC. The same pulse will set the local bit counter (FS 2) to the state of 31 and will set the bit designated C in the local shift register in bit location 24. With a positive synchronizing pulse present on terminal 6 of circuit B1 and flip-flop MS set, a negative pulse will be present on terminal 1 of circuit B1. This pulse changes the state of flip-flop SS from a reset to a set state, causing the data receiver to change from an idle to an active data receiving mode. Each bit slot to follow is an active piece of data, and pulses will appear as 0s and 1s on terminals 0 and 1 of circuits B0 and B1. With the counter (FS 2) changed to a set state, terminal 27 of circuit STC goes high and positive pulses are generated on terminal 27 of circuit BC each time a pulse is present on terminal 27 of the SYNC. The bit counter is advanced each time a bit slot has passed, and the data receiver continues in this manner until the counter indicates the end of a word.

1.07 An initial 1 (or if in the active mode [flip-flop SS set] either a 0 or 1) will be gated through B0 or B1 and the SH gates to lead SH. This causes a negative pulse on lead SH. These shift pulses will advance the local shift register (FS 3) at 0-crossing times of the local 700-Hz oscillator. Each time a mark has been detected and a negative pulse has been generated on terminal 1 of circuit B1, the local parity bit counter will be advanced. The received data word is expected to have an even parity so that at the end of a transmitted word, the parity bit counter is in a reset state. This is verified at the instant the data receiver returns from an active to an idle mode. With the data receiver idle and the parity bit counter reset, no signals will be present on lead ASW. If, at the instant the data receiver is made idle, the parity counter is in its set state, lead ASW will go low and indicate the discrepancy in the state of the local parity bit counter. This ASW signal is connected to the shift register (FS 3) and is conveyed to the transmitting circuitry in the central office by the local data transmitting circuit. The data receiver expects to see 26 bits, including the start bit. At the time the local counter has counted through its state of 26, lead TR goes high and terminal 27 of circuit STC will go low to stop further counting. The data receiver circuit samples the line signal in the center of each bit slot. When a mark is found, flip-flop MS becomes set during the center of a bit slot. The 0-crossing synchronizing pulses serve as an interrogated pulse of the state of flip-flop MS.

1.08 The initial mark is recognized by the data receiver and appears as a pulse on terminal 1 of circuit B1. This information is sent to the shift register (FS 3) and is regarded as the first bit that has been received. Therefore, at the end of transmission, a 1 should be present in the highest numbered bit position in the shift register, bit position ST on FS 3. At the end of transmission, bit position ST remains in a set state until the local bit counter (FS 2) resets it by advancing to the state of 26.

2. BIT COUNTER - FS 2

2.01 The primary purpose of the bit counter is to determine the end of a transmitted word. The counter will, when it assumes the state of 25, cause a negative dc shift on terminal 1 of circuit T25. This action changes the data receiver (FS 1) to an idle mode. The counter advances to the state of 26. One more time slot has elapsed during which the state of the parity counter (FS 1) is being checked

and the state of the ASW information has been determined. At the counter state of 26, the leading bit position of the shift register (FS 3) is forced into a reset state and applies a steady 700-Hz tone to the line. Any further advance of the counter is inhibited by lead TR going high.

2.02 The bit counter also contains tone gate TG. This is the circuitry needed to apply signals to a line and transmit data to the central office. If the location of the central office is 1 mile or more (loop resistance greater than 400 ohms) away from this centrex unit, then the line is connected to the tone gate on terminals 3 and 9. If the central office is less than a mile from this centrex unit, delay is introduced in the data loop by connecting the line to terminals 25 and 1 of the tone gate with terminals 0 and 2 connected to terminals 3 and 9. The data that is transmitted to the central office is in synchronization with the data receiver and is determined by the content of the local shift register (FS 3). The leading bit position of the local shift register is connected to terminals 24 and 27 of the tone gate over leads designated 0 and 1.

2.03 The tone gate should connect to a 900-ohm line. Tone levels applied to the line will not exceed -2 dBm.

3. SHIFT REGISTER - FS 3

3.01 The shift register stores the received data word. A negative pulse on common lead SH will shift the content of the register one position. All cells of the shift register may become reset by a negative pulse on common lead RES.

3.02 The shift register, in its primary application, stores the received data word until the connected lamp control circuit has acted upon the data and returned a pulse on lead RES. The leading position of the shift register connects to the tone gate on FS 2. The tone gate controls the application of a signal to the line which transmits the content of the register during the time the circuit is active. The shift register provides temporary storage for key-signal information which may be inserted into the shift register in parallel form over the leads (1, 2, 4, 8, 16) that connect to the cells. When a key signal is inserted into the register, bit location 20 is also set and is regarded as a key signal presence flag.

3.03 When the local data receiver detects the presence of a start signal, bit position C is set over lead SC. At the first following 0-crossing time, this set state of C will be advanced to bit location ST. This insures that the leading bit location changes its state in synchronization with the local transmitter.

3.04 The change from reset to set changes the transmitted signal from continuous space signals to an initial mark. This is a recognition signal to the central office circuitry that the data receiver (FS 1) has properly responded to the initial mark. After 26 bits of data have been received, register ST location will be set and will indicate the initial mark recognized at the start of transmission. This set state is allowed to remain in this cell unless lead ASW is pulled low. After the data receiver and transmitter have assumed an idle mode, an additional single bit of information is transmitted to the central office during the time the local bit counter (FS 2) is in the state of 25. This additional bit is expected to be a mark signal unless a discrepancy has been found in the state of the local parity bit counter. In such a case, lead ASW will change the state of location ST immediately after the bit counter has reached the state of 25. The state of the local parity bit counter is conveyed to the central office as a mark or a space signal. At the state of 26 of the local bit counter, lead RLB is low, and location ST is forced to assume a reset state, applying a steady space signal to the line. These signals are all applied by the tone gate on FS 2.

4. KEY SIGNAL PRESENT CIRCUIT - FS 4

4.01 A key may be operated on an associated centrex attendant console. The identity of the key is determined by the way in which the negative pulse on the CK( ) lead is routed through the translator (FS 5). This unique identity is a 5-digit binary number (00001 to 11110), which is loaded directly into the shift register (FS 3). This action can only take place if the data receiver and associated lamp control circuitry are idle, as determined by the RR gate and the RR relay.

4.02 Four console control units may be associated with the data receiver. Each control unit has its own signal-source generator (to drive the CK lead), which basically consists of relay K32. The operation of a key applies battery through a resistor on one of the diode-translator packs to the CK lead, then through inductor L10, R32, K32, and CR4 to ground. This causes relay K32 to operate. It also puts lead CK at about a +15 volt level. Prior to this action, capacitor C31 is changed to +24 volts (through R33). As the make contacts of K32 close, the positive side of C31 is terminated to ground through CR6 and contacts on relay RR. A negative pulse is superimposed upon the 15-volt dc level on the CK lead. This negative pulse will go below ground by approximately 8 volts.

4.03 A similar negative-going pulse, caused by capacitor C34, will propagate through CR2 to set flip-flop KSP. This operates the KSP relay which signals "key signal present" over the dc phantom loop (R37, leads CT0 and CT1, and break contacts of relay RR). This signal is a request for the central office to initiate a transmission. It also sets bit 20 in the register (FS 3), which signifies that the word then in the register is a key signal. Load resistors on terminal 7 of the KSP flip-flop prevent noise from setting the flip-flop erroneously, and supply enough current through the R34s to keep the CK lead and that side of C31 at a normal (no keys operated) +10 volts. Diode CR6 prevents a charged C31 in a different control unit from discharging into a recently discharged C31. This can happen when two keys on different consoles are pushed several milliseconds apart. However, if the register is active at the time, two or more consoles could load key signals into the register simultaneously after it is idled.

4.04 Flip-flop KSP is reset the instant the circuit changes from idle to active. If the console key is operated at a time when the circuit is busy, relay K32 will operate, but the termination to ground through the contacts of relay RR will be absent, and the key signal will be delayed until the data receiver is idle and the register is reset.

4.05 Leads LSP and INT connect to the centrex attendants console lamp control circuit. They are used to inform that circuit that either a lamp signal is present in the shift register (FS 3) or that an interrogate request is being made and that the various bits of information pertaining to the request are to be loaded into the shift register.

4.06 If information bit 20 is set, bits 21 and 22 are reset, KSP flip-flop is reset and the data receiver is idle, terminal 27 of circuit R20 will go low and reset bit 20. This insures that bit 20 by itself cannot remain set unless the key signal present flip-flop (KSP) is set.

5. CONSOLE KEY TRANSLATOR - FS 5

5.01 This circuitry uses diode translators to encode a specific console key identity when a key is pushed. The combination of battery and resistors keeps the associated leads held high under idle conditions to prevent false setting of register cells. When a key is pushed, current from these resistors can flow into the key signal present circuit (FS 4) to operate K32.

5.02 Each console control circuit is assigned its separate group of 5 bits for identifying its 32 keys. For example, shift register (FS 3) cells 0 through 4 identify keys on console 0. The position of the information in the register word identifies the console with which the key is associated. There can be no all-zeroes key information, nor is there any parity check on key information.

6. DESCRIPTION OF OPTIONS

6.01 Two alternative options (options Y and Z) pertain to the data loop cable length and directly control the use of a pad located on the tone gate circuit pack. Wiring associated with these options is done on the terminal strip, TS(A0), on top of the cabinet. Refer to CAD 5 (Sheet G9) or T*1E059 (Sheet A3). These options must be closely coordinated with options in the central office connecting circuit (SD-1A265-01). Refer to SD-1A265-01 and the working limits of SD-1E059-01 (Sheet D1). Due to the effects of different loop lengths on the phase relationships of oscillator at the central office end (or actually the relationship between the shifting and input gating of that register), the total loop delay must be incrementally varied depending on its physical strength.

6.02 Option X (the C35 capacitor 596G, 1.96 UF) prevents erroneous ASW failure indications. On installations with battery backup, which do not have the added filtering provided by the ac rectifiers mounted in the cabinet, noise caused by relays releasing at the end of a lamp order execution interferes with the line amplifier circuit pack. This causes a 1 to be detected and results in transmission of a single 1 back to the central office. This 1 is then interpreted as indicating an ASW failure.

6.03 Options W and V (the C31 capacitor 542A, 0.5 UF and C31 capacitor 542D, 1.0 UF, respectively) are alternative options which pertain to the cabinet-to-console distance. The maximum recommended cable length is 1000 feet. Since the original design of 0.5 UF provides only marginal drive to the CK lead (FS 4), this would result in occasional erroneous key signals. Therefore, 1.0 UF (option X) is recommended for use on cable lengths of over 500 feet.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Maximum external loop resistance is 1500 ohms.

1.02 Maximum external loop length is 45,000 feet.

2. FUNCTIONAL DESIGNATIONS

2.01 Miscellaneous

Designation	Meaning
ASW	All-Seems-Well
AT	Analog Timer
B0	0 Bits
B1	1 Bits
BC	Bit Counter
C	Control (Bit)
C25	Count of 25
C26	Count of 26
CK	Console Key
CT0	Center Tap 0
CT1	Center Tap 1
H	High
INT	Interrogate
INV	Inverter
KSP	Key Signal Present
L	Low
LA	Line Amplifier
LSP	Lamp Signal Present
LSS	Line-Signal Sampler
MS	Mark and Space
OBC	Oscillator Buffer Circuit
OSC	Oscillator
PC	Parity Count
PG	Parity Good
R	Ring
RES	Reset
RLB	Reset Leading Bit
RR	Register Reset
SC	Set Counter
SG	Shift Gate
SH	Shift
SS	Start-Stop
ST	Start
STC	Start to Count
T	Tip
T25	Time Slot 25
T26	Time Slot 26
TG	Tone Gate
TR	Transmit
SYNC	Zero-Crossing Sync Generator

3. FUNCTIONS

3.01 Recognize mark and space signals in the received line signal based upon a predetermined method of signaling.

3.02 Accept mark and space signals at a rate of 1400 BPS.

3.03 Provide means for transmitting the content of a local shift register in synchronization with the received data.

3.04 Provide means for recognizing key signals and identifying key numbers.

3.05 Place a request on the data loop to initiate transmission and to transmit the key identity stored in the local shift register.

3.06 Provide means for recognizing the start and determining the end of a transmitted data word.

3.07 Provide means for determining proper parity of the received word and transmitting the result of the parity match to the central office.

3.08 Provide means for detecting the absence of signals on the incoming line.

3.09 Provide means for resetting the shift register, returning the circuit to an idle state.

3.10 Signal the lamp control circuit that a lamp order or interrogate order has been received.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed:

(a) Centrex Data Link Circuit - SD-1A265-01.

(b) Centrex Attendant Console Lamp Control Circuit - SD-1E063-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are specified in the X-77718 specification.

SECTION IV - REASONS FOR REISSUE

B. Changes in Apparatus

B.1 Added

C35 Capacitor 596G, 1.96 UF, Option X - App Fig. 1

B2.

Superseded	Superseded By
C31 Capacitor 542A, 0.5 UF, Option W - App Fig. 3	C31 Capacitor 542D, 1.0 UF, Option V - App Fig. 3

D. Description of Changes

D.1 A 1.96 UF capacitor was added on an optional basis (option X) as a filter on the +24 lead at the line amplifier. This capacitor should be used on all installations which have battery backup (105-E), especially if ac rectifiers are not used in the cabinet. Noise on the +24 lead can cause an ASW failure indication to be sent back to the CO.

D.2 The value of capacitor C31 was changed from 0.5 UF to 1.0 UF. The 1.0 UF capacitor (option V) is satisfactory for any length of cabinet-to-console cable.

The 0.5 UF capacitor (option W) is not recommended for cable lengths of greater than 500 feet. The larger capacitor provides the added drive necessary for setting bits in the register in the presence of the higher capacity loss in long cables.

D.3 Drawing changes were made to clarify options Y and Z associated with the delay pad on the A345 pack. Also, trouble-shooting waveforms and block diagrams were added to the H section.

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