6

COMMON SYSTEMS COMBINED SCANNER AND SIGNAL DISTRIBUTION MATRIX CIRCUIT

CHANGES

D. Description of Changes

D.1 CAD 6 has been changed to indicate the correct wire gauges required for connection to the power terminal strip.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5251-JWD-RSP-DA

COMMON SYSTEMS
COMBINED SCANNER AND
SIGNAL DISTRIBUTION MATRIX
CIRCUIT

CHANGES

D. Description of Changes

D.1 CAD 5, CAD 8, and FS1 have been corrected to clarify wiring information to agree with design intent and manufacturing drawings.

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DEPT 5251-JWD-RSP-DA

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The scanner portion of this circuit transforms electromechanical contact opens and closures with or without resistance battery into digital logic TTL levels.

1.02 The scanner voltage transform is provided by individual scan networks which consist of a 3-resistor divider, a filter capacitor, and an integrated circuit TTL multiplexer.

1.03 The scanner networks are organized in a 16 word by 10 bit matrix (160 points) that is accessed by a binary address.

1.04 The states of the scan points in the row (word) selected by the address read-out as 10 bits of data.

1.05 The distributor portion of this circuit interfaces 5-volt digital logic TTL to electromechanical circuits by means of mercury relays.

1.06 The distributor mercury relays 337A are driven directly from TTL logic since they operate from 5 volts.

1.07 A clean make-contact is provided for each relay as the signal distributor point.

1.08 The state of each relay is controlled by a latch. The output of the latch drives the relay coil via a buffer type TTL gate.

1.09 The signal distributor is organized in a matrix of 24 points (4 words by 6 bits).

1.10 The state of the distributor points in a row (word) is controlled by the address and 6 bits of data.

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2. GENERAL DESCRIPTION OF OPERATION

2.01 A scanner/distributor constructed from these units would consist of a minicomputer or processor, an interface to its I/O bus, and from 1 to 16 of these units. The interface provides an interunit bus to which the scan/distribute units are connected. This system can be expanded beyond 16 units by providing additional interfaces.

2.02 This circuit receives an 8-bit address, a control bit, a master sync signal, and 16 bits of data from the processor via the I/O interface. All units on the bus receive the same information, however, only one will recognize the 4-bit name (high-order address bits). When the control bit is in the read state, the named unit will return 16 bits of data from the row of scan points selected by the low order 4-address bits and a slave sync pulse. When the control bit is in the write state the named unit will write the 16 bits of data into the row of latch selected by the lower order 2-address bits and return a slave sync signal. It should be noted that address bits 3 and 4 are ignored on a distribute and thus each distribute row will respond to 4 separate addresses.

SECTION II - DETAILED DESCRIPTION

1. INTRODUCTION

1.01 The combined scanner and signal distributor circuit consist of a 24-point distribute matrix (4 words by 6 bits), a 160-point scan matrix (16 words by 10 bits), and a controller circuit pack to interface the matrices to the interunit bus.

2. SIGNAL DISTRIBUTOR MATRIX

2.01 The matrix consist of three A1074-type circuit packs (DM0-DM2). Each circuit pack contains eight signal distributor points organized as 2 bits of four words. The two low-order address are decoded into four clock signals which select a unique word out of the four.

2.02 Data received from the bus is written into the row (word) of latches selected by the active clock signal. All distributor matrix packs are clocked simultaneously to affect a 6-bit write operation.

3. SCAN POINT MATRIX

3.01 The matrix consist of ten A1068-type circuit packs (SM00-SM09). Each circuit pack contains 16 scan points organized as 1 bit of 16 words. The low-order address bits select a unique word out of the 16. All matrix packs are addressed simultaneously to affect a 10-bit read operation.

3.02 The binary information from the scan points is gated directly onto the data lines of the interunit bus. The interunit bus drivers have enables so that the data is gated only when the controller decodes a scan.

3.03 The matrix pack contains two 8-line to 1-line data selector/multiplexers. These integrated circuits use the lower order four address bits to select 1 of 16 scan points to be read-out onto the bus. The 5-volt power for these ICs is gated (strobed) by the controller pack. Power is applied to the selection logic only when data from the scan points is to be read-out.

3.04 The scan point network is designed to interface electromechanical circuits to digital logic with ground differentials of 0 to 5 volts and still provide adequate operating margins.

4. SCAN/DISTRIBUTE CONTROLLER

4.01 The scan/distribute controller (A1075) receives 8-address bits, a control bit, and a master sync pulse from the interunit bus. The higher order 4-address bits are compared to a 4-bit name field wired directly on the circuit pack connector. If the address present on the bus matches the wired name, then this unit will return a slave sync signal 4 gate delays after receiving the master sync signal. If the control bit is a logical "0" (read cycle), the controller will send the lower-order 4 address bits to the matrix and generate the power strobe and bus enable signals. If the control bit is a logical "1" (write cycle), the controller will generate a 1-out-of-4 clock signal determined by the lower-order 2 address bits. The clock signal loads the data received from the bus into the latches on the matrix packs. The bus receivers are enabled at the same time the slave sync signal is generated.

5. BUS CONNECTORS AND TERMINATORS

5.01 The interunit bus is equipped with a pair of connectors labeled IN and OUT. The IN and OUT connectors are strapped together so that the bus can be continued from one unit to the next. The OUT connector for the last unit on the bus is used for the bus terminator.

5.02 The bus terminator is a resistor divider for each signal on the bus and establishes the inactive voltage level. This leve is a 'high' voltage of 3.0 to 3.8 volts depending on the tolerances. The bus active level is a 'low' voltage of 0 to 0.4 volts depending on the saturation voltage of the device driving the bus.

5.03 The resistor dividers in the bus terminator requires 5 volts which is supplied to the OUT connector from the unit battery terminal.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Voltage Limits

Voltage	Desig	Min	Max
+ 5	AB	4.5V	5.5V
-48	AA	42.75V	52.50V

1.02 Temperature Limits

Operating temperature range is 0 to 50° C ambient.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Packs

Designation	Meaning
SC0	Scan/Distribute Controller
SM00-SM09	Scan Matrix 00 through 09
DM0-DM2	Distribute Matrix 00 through 02

2.02 Signal Heads

Interunit Bus Signals

Designation	Meaning
A0-A8	Address Bits 1 through 8
C1	Control Bit 1
D00-D15	Data Bits 00 through 15
MSYN	Master Sync
SSYN	Slave Sync

Note: The interunit bus signals are negative logic; a logical '1' is a low-voltage of 0 to 0.4V: a logical '0' is a high-voltage of 3.0 to 3.8V.

Intraunit Signals

Designation	Meaning
AD1-AD4	Matrix Address Bits 1 Through 4
N5-N8	Name Field Bits 5 Through 8
STRB	Scan Matrix Power Strobe
CLK0-CLK3	Clock Row 0 Through 3
EN	Enable Bus Drivers

Scan Inputs

Designation	Meaning
SC0000-SC0009	Scanner Row 00 Bits 00 Through 09
SC0100-SC0109	Scanner Row 01 Bits 00 Through 09
SC0200-SC0209	Scanner Row 02 Bits 00 through 09
SC0300-SC0309	Scanner Row 03 Bits 00 through 09
SC0400-SC0409	Scanner Row 04 Bits 00 through 09
SC0500-SC0509	Scanner Row 05 Bits 00 through 09
SC0600-SC0609	Scanner Row 06 Bits 00 through 09

2.02 Signal Heads (Contd)

Designation	Meaning
SC0700-SC0709	Scanner Row 07 Bits 00 through 09
SC0800-SC0809	Scanner Row 08 Bits 00 through 09
SC0900-SC0909	Scanner Row 09 Bits 00 through 09
SC1000-SC1009	Scanner Row 10 Bits 00 through 09
SC1100-SC1109	Scanner Row 11 Bits 00 through 09
SC1200-SC1209	Scanner Row 12 Bits 00 through 09
SC1300-SC1309	Scanner Row 13 Bits 00 through 09
SC1400-SC1409	Scanner Row 14 Bits 00 through 09
SC1500-SC1509	Scanner Row 15 Bits 00 through 09

Signal Distributor Outputs

Designation	Meaning
D000(A,B) - D005(A,B)	Output Pair - Row 0, Bits 00 through 05
D100(A,B) - D105(A,B)	Output Pair - Row 1, Bits 00 through 05
D200(A,B) D205(A,B)	Output Pair - Row 2, Bits 00 through 05
D300(A,B) - D305(A,B)	Output Pair - Row 3, Bits 00 through 05

2.03 Connectors

Designation	Meaning
IN	Bus Input Connector
OUT	Bus Output Connector

3. FUNCTIONS

3.01 Provide a matrix of 24 signal distributor points (4 rows by 6 bits).

3.02 Provide a signal distributor point that consists of a 5-volt digital logic TTL latch, relay driver, and mercury-wetted relay 337A.

3.03 Write a row of latches selected by a binary address with 6 bits of data.

3.04 Provide a matrix of 160 scan points (16 words by 10 bits).

3.05 Provide scan point networks that translates relay contact opens and closures into digital logic levels.

3.06 Read any row of scan points with a binary address.

3.07 Provide a 4-bit name field which allows up to 16 of these units to be connected to a common interunit bus.

3.08 Provides a slave sync signal if the unit is functioning properly.

4. CONNECTING CIRCUITS

4.01 None.

5. MANUFACTURING TEST REQUIREMENTS

5.01 The Manufacturing Test Requirements are specified in the X-78994 specification.

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