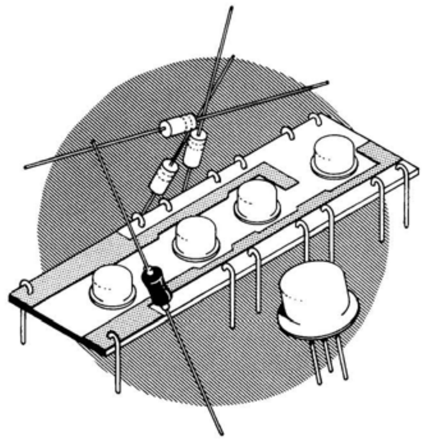
SOLID STATE DEVICES

Handling and Selection Guide

Western Electric
MANUFACTURING & SUPPLY UNIT OF THE BELL SYSTEM

SOLID STATE DEVICES

Handling and Selection Guide



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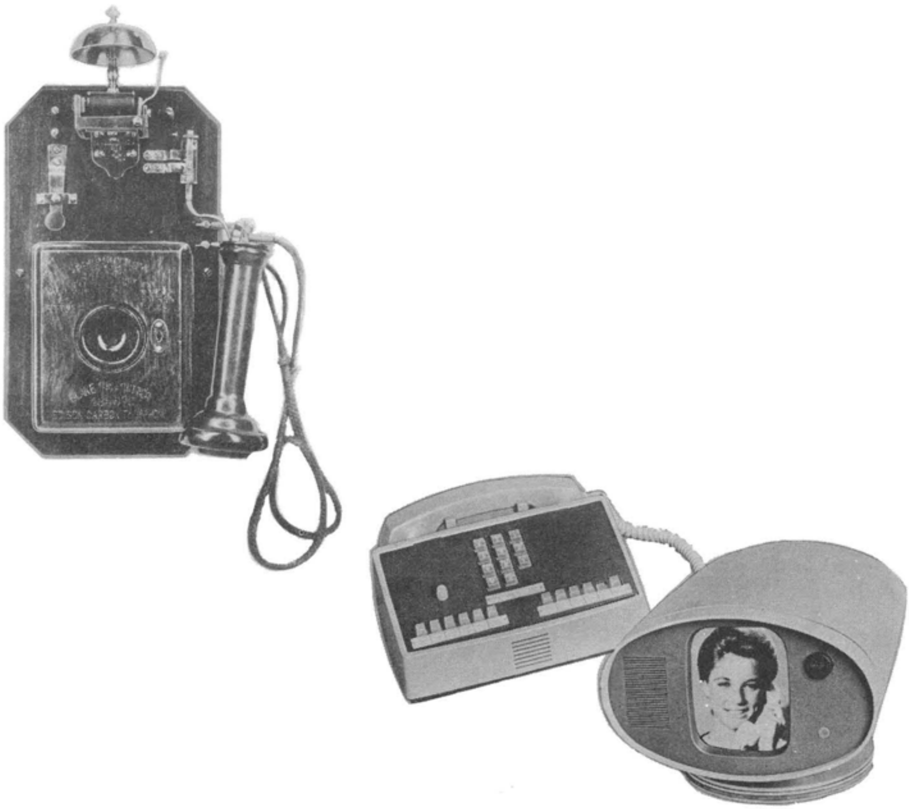
Introduction

In 1948, Bell Telephone Laboratories scientists announced a tiny new device which was destined to change the world of electronics. Called the transistor, its ever growing family of solid state devices is already providing greatly improved telephone service and offers the promise of many more exciting developments in the future.



Success of the telephone system is dependent upon devices having high reliability at a reasonable cost. Reliability results from good design, controlled manufacturing processes, and wise selection and handling of the devices.

The active region in a miniature electron tube is approximately a million times greater than the volume of the active region of a typical switching transistor. An appreciation of this scale difference is important in translating conventional electron tube practices to solid state devices. The key to obtaining stable electrical characteristics in a transistor or diode is a surface cleanliness of semiconductor material junction to an atomic level. Maintaining this cleanliness over a very long period of time is the function of the device package or surface passivation.

The device user must therefore appreciate the minuteness of the active region, the cleanliness level established by the manufacturer and the importance of protecting the soundness of the package seal. Lack of such appreciation can lead to degradation of the essential built-in reliability and to the possibility of placing potential defects into circuits doomed to fail in service.

Solid state devices on which our present and future telephone systems are so greatly dependent are expected to operate reliably for many decades. However, a very small percentage of these devices could have a limited life because of improper manufacture or use. These are of great concern because they limit the ultimate reliability of the system in which they are used.

It is the purpose of this book to help the user protect this reliability by setting forth suggestions for the handling of the various solid state devices and making the user more knowledgeable of the devices and why they were selected for their particular application.

INTRODUCTION

After World War II, the Bell Telephone Laboratories at Murray Hill, New Jersey, applied considerable effort to the development of a solid state amplifying device using semiconductor materials such as germanium and silicon. It was known in the mid-forties that such materials possess mobile carriers of charge that move under the influence of an electric field resulting in a current. It was also known at this time that two different types of carriers were possible. For example, germanium and silicon atoms possess 4 electrons which could combine chemically, (valence of 4). If some of their atoms were replaced by atoms that have a valence of 5 (for example, phosphorous or antimony), then the extra electrons would be loosely held in the crystal and be relatively free to move about. This forms the n-type crystal. If some atoms of the semiconductors were replaced by a valence three element such as aluminum or boron, then within the crystal structure electrons would be missing. These are called holes which are easily filled by electrons from neighboring atoms. In the process of filling a hole, a new one is created. This process can take place in particular directions depending upon the applied voltage and thus form a current of positive charge. The semiconductor doped in this manner is called p-type.

Early experiments attempted to change the conductivity of a doped semiconductor by the action of a charged plate immediately above its surface. This is similar to the familiar electroscope or cat's fur experiments in elementary physics. It was hoped that a little power on the plate could control considerably more power by changing the conductivity of a semiconductor bar. The results with the charged plate were insignificant but by trying to increase the effect of the field using points instead of plates, the point contact transistor resulted when one of two points, as shown in Figure 1, was "formed" by the passage of current. As was later proved, the phosphorous in one of the point contacts was the important ingredient for collector operation and hence amplification.

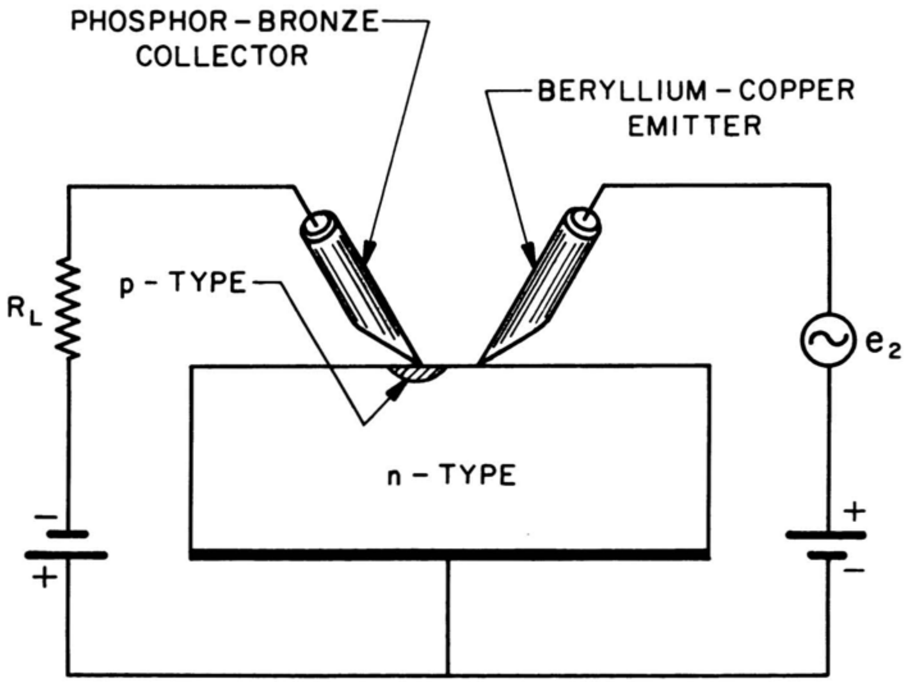
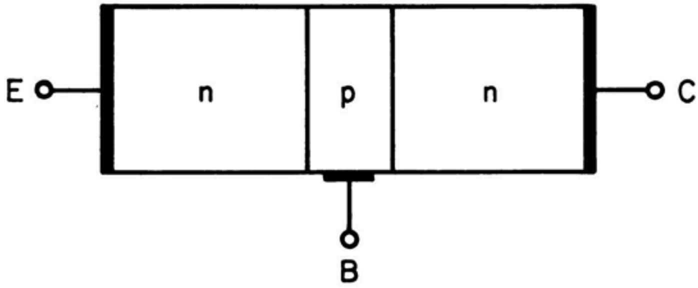
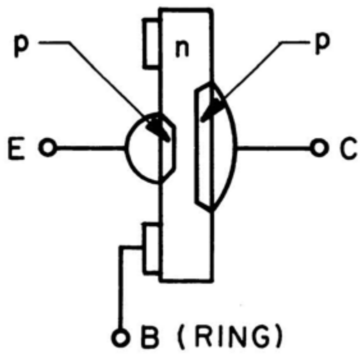


Figure 1.

As a result of the experience gained from the point contact transistor and from a better understanding of junctions formed by n- and p-type regions, the junction transistor was developed two years later. Figure 2 shows the two junction-types which were developed at this time.



GROWN JUNCTION



ALLOY JUNCTION

Figure 2.

One type was grown by pulling a seed crystal out of a pool of molten semiconductor material which was alternately doped by n and p impurities. The other was alloyed by melting metal buttons on alternate sides of a wafer and doping the crystal in the resolidification process.

Although point contact transistors remained superior in frequency responses, these junction devices had definite advantages in that they were capable of handling larger power, were less noisy, were easier to handle in circuits, and had a more controllable manufacturing process.

Even though solid-state diodes have a much earlier history, going back before the turn of the century, the invention of the transistor led to a parallel improvement and development of the diode art. This naturally resulted from the intensive effort which went into the better understanding of device physics and materials, and the development of fabrication techniques. Since the diode, with the exception of special types such as the tunnel diode, the gold bonded diode, the regulator diode etc., is essentially a device possessing only two of the three regions of a transistor, it will not be treated as a separate device in this section.

The mid-fifties proved most important in the history of the transistor. In 1955, the diffusion technique was introduced in the junction transistor fabrication process. Thus, under the application of a gas or surface deposition of materials possessing proper impurities, doped regions were formed by the application of heat. These regions which can be controlled to a depth of less than ten billionth of an inch, then allowed for junction transistors to enter the 100 to 1000 megacycle range. The diffusion technique not only led to a break-through in the frequency response of junction transistors but also introduced a batch-type process which was to become the basis of modern transistor technology. Thus, thousands of transistor elements are handled simultaneously through most of the processing reducing greatly the need for individual operations. This also allows for greater uniformity in the product. Figure 3 shows a cutaway section of a diffused base mesa transistor element.

The next significant improvements took place at the end of the fifties with the introduction of the planar epitaxial transistor, as shown in

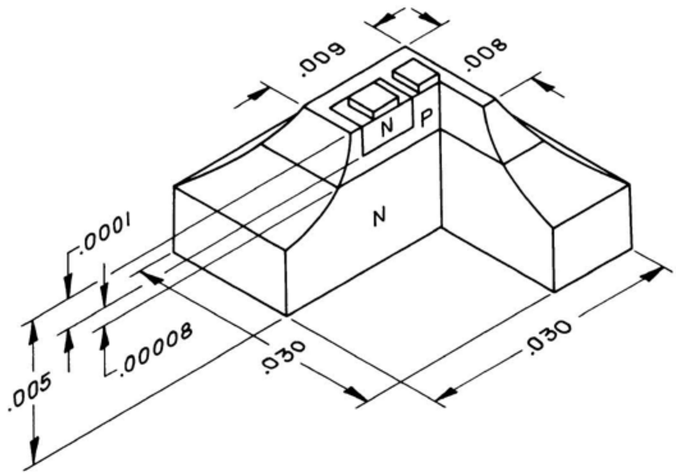


Figure 3.

a cutaway representation in Figure 4. By growing the desired crystal on a heavily doped substrate, as shown by the n+ region, an improved device, particularly for switching applications is formed. The new

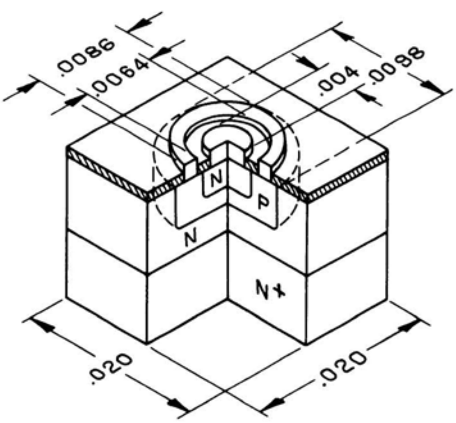


Figure 4.

structure allows for many improvements, particularly higher voltages while still retaining the desired low "on" voltage and switching times.

The planar technique, which eliminates the older mesa formation, also permits close control and reproducibility of junction regions through photographic techniques. The planar structure (i.e., the top surface being flat or planar) also eliminates the problem of interconnections between active elements in the same slice; this was important to solid integrated circuits which soon followed.

Figure 5 shows a monolith integrated circuit using beam leads. Interconnections are made by the "batch process" of evaporation. Thus, good designs and process controls yield circuits which can be made at lower cost than their counterparts using individual components.

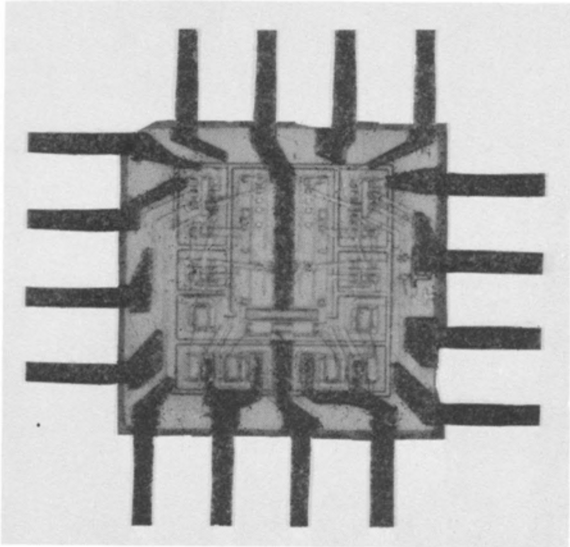


Figure 5.

DEVICE DESCRIPTION

A device giving promise of low cost and good performance, the "Beam Lead" transistor was introduced in the mid-sixties. A single beam lead device is shown in Figure 6.

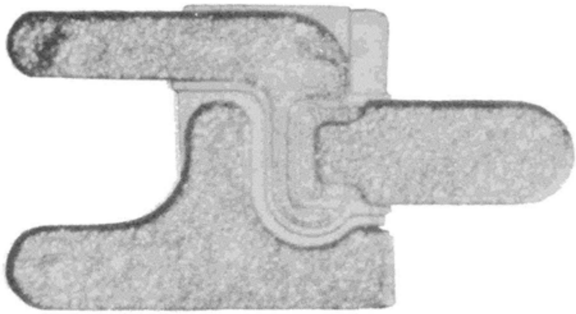


Figure 6.

These devices possess protective coverings across critical boundary regions as well as heavy leads which facilitate the connection problem. The appearance of the relatively thick leads led to the name of "Beam Lead". In order to prevent harmful results of scratches and dust, a relatively simple enclosure can be provided.

Another solid state technique which gives promise of large usage in the Bell System is Thin Film Circuitry. By the use of the refractory metal tantalum, capacitors, resistors and interconnections are all produced in a single pattern on smooth glass or ceramic substrates. With the application of semiconductor devices in the form of Beam Leads, single components or integrated circuits, the circuits which are formed are reproducible and low in cost because of processing which is dependent mainly on photolithographic batch techniques. Figures 7 and 8 show hybrid thin-film circuits using conventional transistors and integrated circuits respectively. The resistors, whose resistance is dependent upon the length, width and thickness of the tantalum film are mainly shown by the "meandering" lines in the Figures.

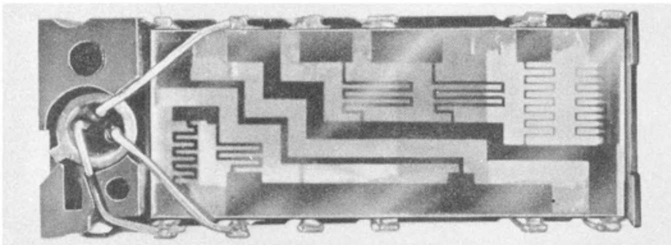


Figure 7.

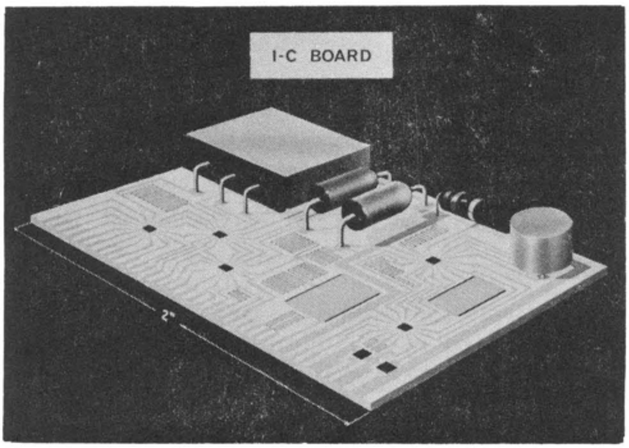


Figure 8.

An interesting review of the historical development which took place in semiconductors and thin films is shown by the tree in Figure 9. The dates in the figure refer mainly to manufacturing dates and not laboratory models or inventions. Some devices were left out in order to simplify the picture. Another interesting story on the transistor

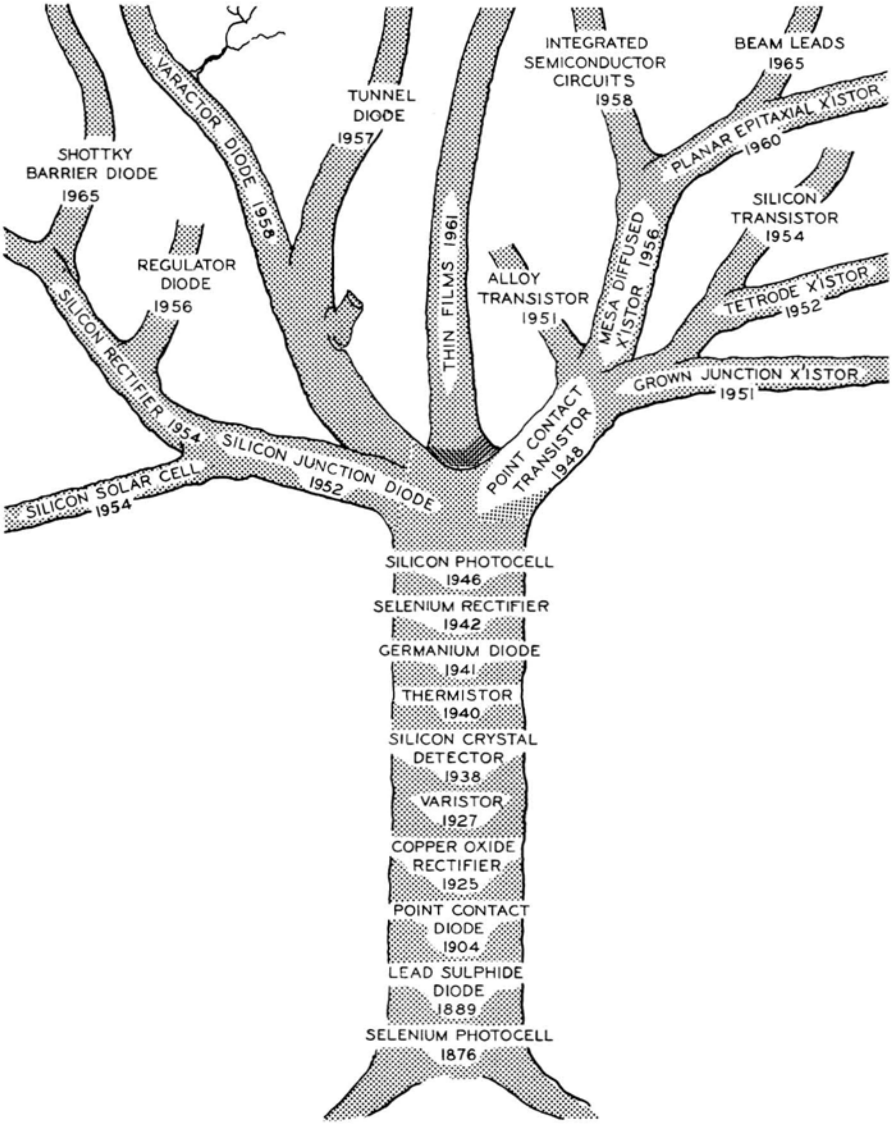

SHOTTKY BARRIER DIODE 1965
VARACTOR DIODE 1958
TUNNEL DIODE 1957
THIN FILMS 1961
INTEGRATED SEMICONDUCTOR CIRCUITS 1958
BEAM LEADS 1965
PLANAR EPITAXIAL X'ISTOR 1960
SILICON TRANSISTOR 1954
REGULATOR DIODE 1956
ALLOY TRANSISTOR 1951
MESA DIFFUSED X'ISTOR 1956
TETRODE X'ISTOR 1952
SILICON RECTIFIER 1954
GROWN JUNCTION X'ISTOR 1951
SILICON JUNCTION DIODE 1952
POINT CONTACT TRANSISTOR 1948
SILICON SOLAR CELL 1954
SILICON PHOTOCELL 1946
SELENIUM RECTIFIER 1942
GERMANIUM DIODE 1941
THERMISTOR 1940
SILICON CRYSTAL DETECTOR 1938
VARISTOR 1927
COPPER OXIDE RECTIFIER 1925
POINT CONTACT DIODE 1904
LEAD SULPHIDE DIODE 1889
SELENIUM PHOTOCELL 1876

Figure 9.

can be shown by Figure 10 which depicts the improvements which took place through the years in the relative cost, frequency response, and reliability. Germanium has always been ahead of silicon in frequency response because of its higher mobility of charged carriers and partly because it was the first material to be investigated. The

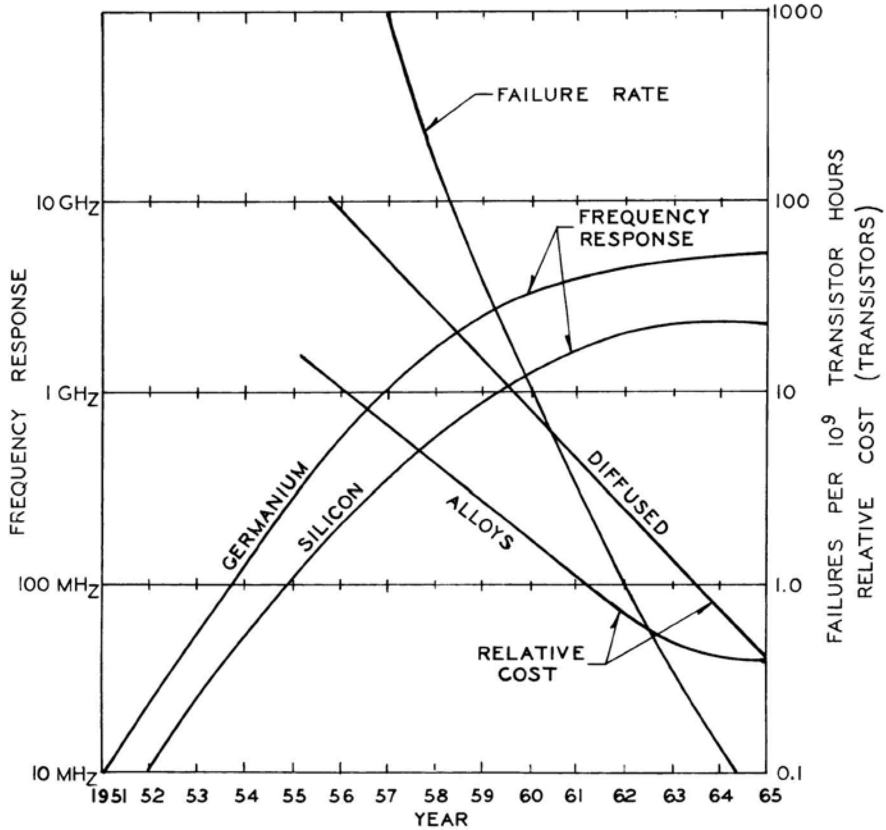


Figure 10.

cost picture for diffused devices will continue to decrease as they are incorporated in solid circuits or as beam leaded structures. Alloy transistors should definitely level out as is shown in Figure 10. The reliability curve, which mainly concerns the high-runner logic devices, was based in large part on accelerated testing results. Good agreement has been obtained from results of large systems such as Nike Zeus, Unicom and No. 1 ESS.

Hybrid thin-film circuits, integrated circuits and beam lead devices all have their places in the future. In some areas a number of acceptable alternatives are possible. It is the mutual responsibility of the circuit designer and the device designer to understand the advantages and limitations of the various technologies and to make a choice based upon the best interest of the Bell System.

CHARACTERISTICS

The purpose of this section is to review in general the characteristics, ratings, and reliability which must be considered in selecting transistors for specific applications. Diodes, in general, would follow similar considerations and, therefore, will not be treated separately.

In general, electronic circuits can be classified into switching or analogue applications. A circuit is called upon to recognize the presence or absence of signals and transmit them at higher levels or recognize various levels and phases of signals and amplify them accordingly. Some applications such as high level amplifiers, mixing, etc., could fall into both categories as well as not be considered at all in these general applications. The differences in the two circuit applications are reflected in the requirements of the transistors. Transistors are specified according to their ability to operate as a switch or as an amplifier. In switching applications dc gain, "on" voltage, "off" voltage, input voltage, high frequency response and storage time, play dominant roles. In amplifying applications, the high frequency response, the power gain, power dissipation, input impedance, and noise figure contribute significantly. In any case, a transistor can be optimized for a particular application. The type of structure (epitaxial or non-epitaxial), horizontal and vertical geomtery, and levels of impurity doping contribute greatly to the optimized design.

Figure 11 shows some of the wafer geometries in our present Bell System devices. It can be seen that the 800 mc transistors, the 44A or 45A type, have a base width W of only about one-fifth that of the 200 mc 16-type. This base width is most important in determining frequency response.

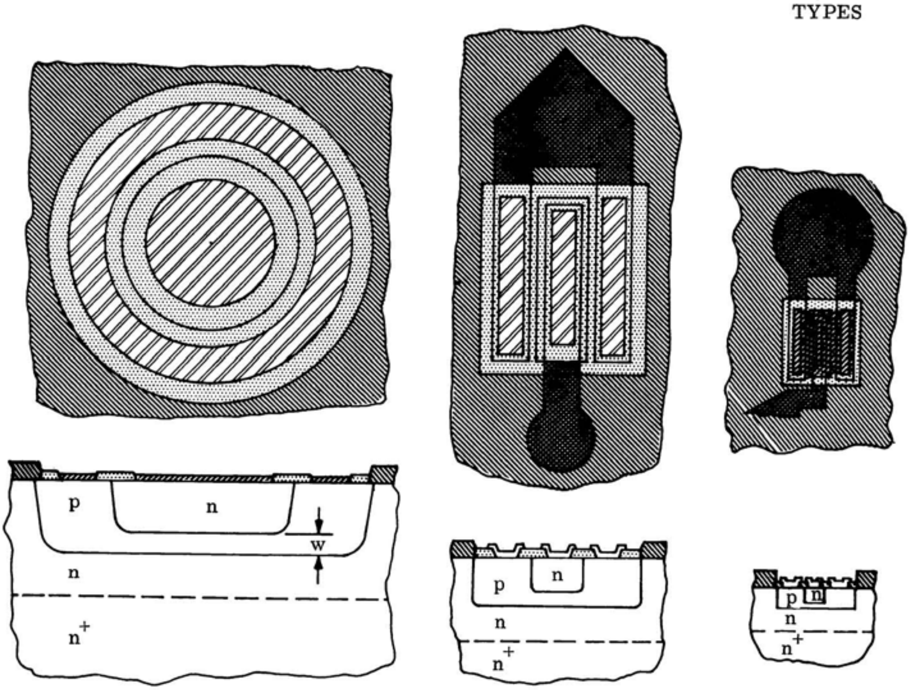


Figure 11.

By paralleling devices internally or redesigning structures by using interdigitation, stars, oak leaves, etc., emitter parameters are increased yielding higher current capability without appreciable loss in frequency response.

SPECIFICATIONS AND DATA SHEETS

The objective of the specification is to assure that the product will satisfactorily function in the circuit. A single specification can guarantee performance, in many cases, in several circuits. The specification must not only assure operation at the beginning but also over the desired life of the equipment and over all necessary ambient conditions. Specifications are prepared for the use of manufacturing locations and data sheets for users. Data sheets supply characteristic curves and data that aid in the designing of circuits. The specification states manufacturing and testing requirements which control the quality of the product and provide the most economic balance of manufacturing and testing control to assure proper performance.

There is little doubt that the cost of manufacture and maintenance is of prime importance to every system designer. It is apparent that minimum costs will be achieved when the specification represents the optimum balance between system requirements, device design, and manufacturing skill. A weakness in any of the three areas can but add to the cost of the system. A mutual understanding between the three areas can greatly help in preventing unnecessary costs.

Some of the important considerations which follow a system from initial development to final manufacture and are necessary for optimum cost are the following:

a. Limit values on test specifications and data sheets must not only reflect temperature and aging variations but must also represent a balance between circuit complexity and performance and maximum device yield. Obviously, limits which are too tight increase costs by increased testing or reduced device yields, while excessively loose limits increase costs by reduced circuit efficiencies.

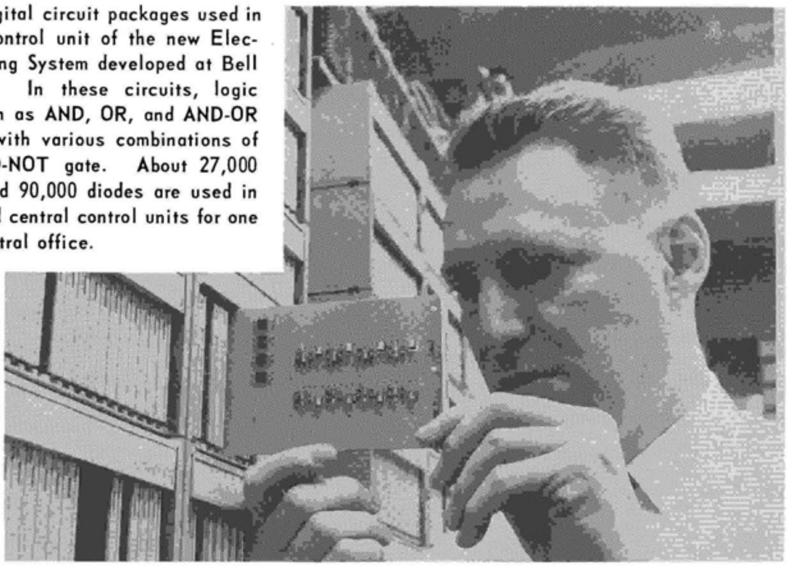
b. Device designs should reflect the latest achievable in electrical performance, reliability, and manufacturability. This can best be obtained by maintaining the areas of design and manufacture at the highest technical level possible and by a constant interchange of information and ideas on new and important product developments and system requirements.

RATINGS AND RELIABILITY

A rating is, by definition, a limit value for a device which if exceeded will impair the expected life of the device. In some cases, the failure can be catastrophic and take place immediately. This generally happens when voltage ratings are exceeded. In other cases the increased degradation will not be immediately apparent but eventually will result in a higher failure rate. This usually results when junction temperature ratings are exceeded.

Handling

With the ever increasing numbers of solid state devices used in today's electronic equipment it is essential that proper handling techniques be employed to insure the overall reliability of the equipment in which they are used. It is the intent of this section to provide these proper handling techniques for the assembly or replacement of solid state devices in such equipment.



One of the digital circuit packages used in the central control unit of the new Electronic Switching System developed at Bell Laboratories. In these circuits, logic functions such as AND, OR, and AND-OR are built up with various combinations of a basic AND-NOT gate. About 27,000 transistors and 90,000 diodes are used in two duplicated central control units for one electronic central office.

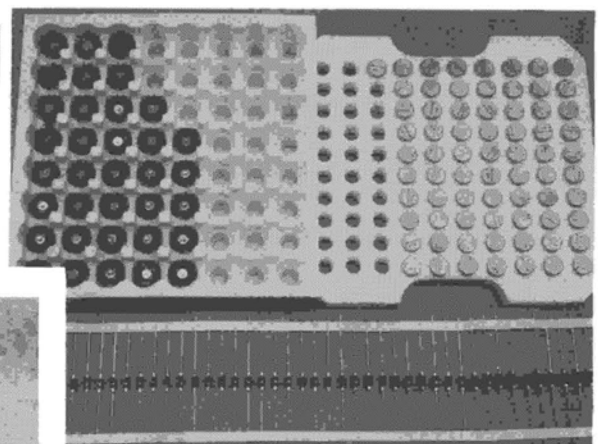
STORAGE

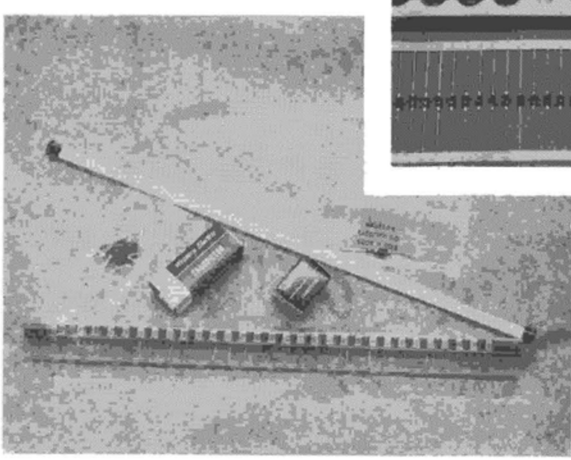
Solid state devices should be stored in their shipping containers whenever possible. These containers are specially designed to give the kind of protection needed. Devices should never be dumped from their cartons into bins. This may result in mechanical shock, cracked glass seals resulting in electrical degradation, and bent or tangled leads, or even scratched leads which are susceptible to corrosion, making soldering difficult. Integrated circuits and hybrid thin film circuits are even more susceptible due to their construction and multiplicity of components. In cases where devices are provided with additional parts, such as lead spacers, mounting washers, thin film insulators and the like, store them with the device to insure their intended use. In general all devices should be used on a "first in - first out" basis. Prolonged storage may cause oxides to form on the leads, necessitating special cleaning before soldering.

PACKING AND UNPACKING

Semiconductor devices may be received packaged in a number of ways depending on the device requirements, manner in which they will be

Multiple Packaged





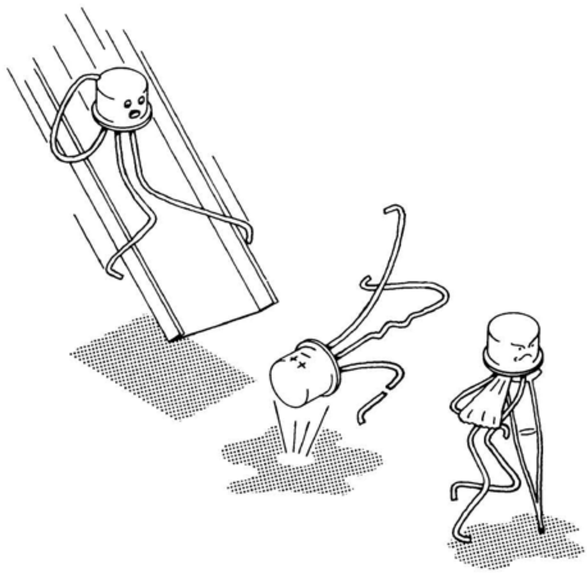
Individually Packaged

used, or even the number ordered. To insure proper packing the devices should be ordered by specifying standard multiple packaging where possible with the remainder individually packaged. For inter-works - locations employing automatic insertion equipment, lead tapes for varistor and diodes and plastic slides and styrene belts for transistors are or will be available. For further information contact the packaging engineer at the producer location. Other bulk packages such as polystrene and styrene vacuum formed Handler-Shipper trays are available. Distributing houses can either order the latter type or in the case of field replacements, individual packaged devices.

If lots must be broken, each group should be repacked in a manner similar to that of the original packing.

MECHANICAL DAMAGE

Semiconductor devices should be handled with about the same care as a glass electron tube if the built in reliability is to be assured. Rough handling or dropping may cause leaks or cracks in the glass seal, damage to the internal wafer (or substrate in the case of thin film circuits), or openings in small internal wire bonds. Although these effects of jolts and jars may not be immediately apparent, they may shorten the life expectancy by causing potential defects. If mechanical damage, such as cracks in the glass seals or substrate, dents in the can (especially the flange), or nicks in the tabulation, is noted, it is recommended that the device not be used. Since thin film circuits are not encapsulated, care must be exercised to avoid damage to the thin film elements. A minute scratch could result in a serious circuit damage. In some cases beryllia is used for mounting washers or device piece parts because of its good heat-conducting and poor



electrical-conducting properties. Care must be exercised in handling this material since it is known to be toxic.

In general, solid state devices are capable of withstanding shocks of the order of 2000g. A fall from a bench to the floor may produce a shock as high as 6000g, depending on the device, the position of impact, and the type of floor surface. Exposure of a transistor or diode to any single jolt or jar may not result in an immediate failure, but shocks in general should be avoided. Microwave point contact diodes, alloy transistors, integrated circuits and thin film circuits are the most susceptible to shock, due to their internal construction.

LEADS

Most semiconductor devices employ a glass-to-metal-seal. The leads of the devices are made with material such as Kovar and Rodar to match the thermal expansion of glass. The number of bends to which a lead may be subjected should be kept at a minimum to assure soundness of the seal. Forcing leads into alignment with terminals or posts by twisting or pulling may damage the seal. All bends should be made not closer than 1/16 of an inch (unless otherwise specified) from the surface of the glass seal or, in the case of plastic encapsulated devices, from the body of the device. Closer bends can result in cracking of the seal, with deterioration of the enclosed environment resulting in lower reliability of the device. The cracks may not be readily apparent even under a microscope.

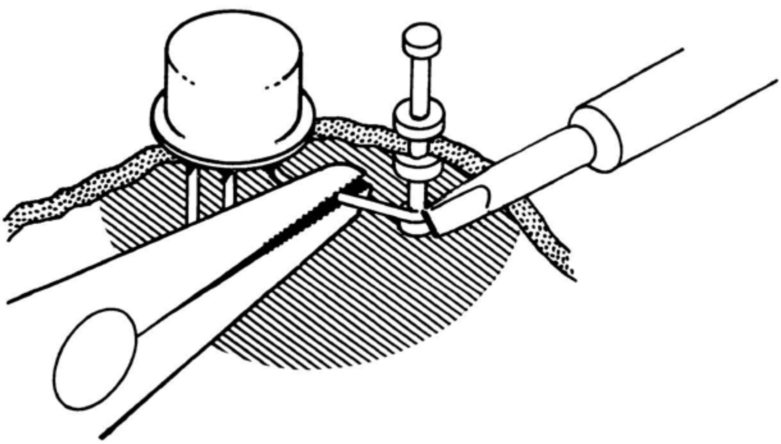
Bent and tangled leads caused by improper handling may result in slow leaks developing in glass seals, or in broken leads or structural changes that would initiate stress corrosion. Handling of leads should be kept to a minimum, as residues from body oils are likely to cause soldering difficulties.

Improper cutting of semiconductor device leads (such as with diagonal pliers), can result in a mechanical shock wave which may travel through the lead into the device and degrade its electrical properties. A shearing tool should be used to minimize the possibility of shock damage. Shears of roughly the same size as diagonal pliers are commercially available and are preferred.

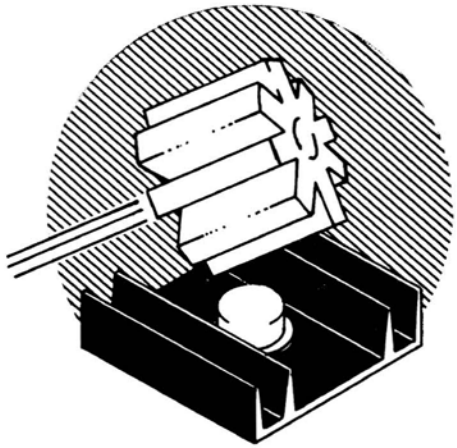
The wirewrapping of semiconductor device leads requires special consideration because of the residual tension and the stress corrosion effects which may develop. This is especially true of gold-plated Kovar or Rodar leaded devices. It is recommended that the appropriate Bell Laboratories Applications Group be consulted before wirewrapping of semiconductor device leads is undertaken. The use of percussion welding is generally not recommended for semiconductor devices, because of the likelihood of damage due to the high currents generated. Resistance welding may be acceptable, provided care is taken to insure that no destructive transients are introduced into the devices. This is particularly applicable to devices which usually have one element connected to the case. Low-power devices, such as ultra-high frequency and NPN alloy transistors, are especially susceptible. The appropriate Bell Laboratories Applications Group should be consulted in regard to wirewrapping or welding techniques.

HEAT SINKS

Heat sinks are classified under two types: (1) the temporary type, which is used in soldering to prevent the introduction of excessive heat to the semiconductor device,



and (2) the permanent type, which is installed with the device to allow a greater dissipation of heat generated within the device itself. The latter can be either a radiator fin-type, which surrounds and is part of the device, or the external type which is mounted to the stud of the



device during circuit assembly. The temporary type will be discussed in the following section on Soldering.

From the electrical standpoint, permanent type heat sinks are used to reduce junction temperature for increased power dissipation capability and reliability. The ability of a semiconductor device to dissipate its rated power is dependent upon (1) internal thermal resistance of the device itself and (2) external factors, such as the size of the heat sink, the thermal resistance between the heat sink and the device, the degree of ambient circulation, and the temperature of the ambient. Device data sheets often contain information concerning these external factors.

The bearing surface upon which a stud-mounted semiconductor device is installed must be flat, clean and free of burrs. This is necessary to insure adequate contact between the heat sink and the device in order to obtain proper heat flow. Thermal contact is improved with a very thin film of silicone lubricant between the clamped surfaces. Care should be used to insure the torque recommended in the data sheets. When electrical isolation is required between the device and an external heat sink, a thin mica or other suitable washer, coated with silicone lubricant, can be used between the two. Care must be taken not to damage the insulating washer.

SOLDERING

A soldering iron, properly connected and grounded may still have leakage voltages present on its tip in excess of 1 volt above ground. This voltage can cause damage, particularly to ultra-high frequency transistors which have emitter-to-base breakdown voltages in the range of 1 volt. With such devices, it is desirable to use a working surface isolated from ground. Some soldering guns, even when adequately grounded, produce transient voltages each time the power is turned on or off. These are caused by the inductive reactance in the tool and ground lead. Particularly susceptible to damage from these transients are NPN germanium alloy transistors, ultra-high frequency transistors, and microwave point-contact diodes.

Wave and dip soldering have an advantage over hand soldering because the entire circuit board is maintained at the electrical potential of the molten solder. Thus, destructive transients are not introduced into the devices. Care must be exercised to insure that solder bath temperatures are uniform, that the duration of immersion is timed properly, and that the devices are not immersed closer than 1/16 of an inch from the glass-to-metal seal. In the case of thin film circuits, time and temperature must be properly controlled to prevent damage to previously soldered connections. Failure to follow these precautions can result in small changes in electrical characteristics which are not easily detected, but which may cause failure of the device. The length of time to which a semiconductor device may safely remain in the molten solder is dependent upon the type (whether alloy or diffused), the temperature of the bath, and the distance heat must flow to reach the critical areas of the device.

Following are some additional recommended practices to use when soldering solid state devices:

1. Higher solder bath temperatures for a shorter time are preferred for better solder-wetting of the leads, and to prevent long heat exposure from affecting the critical areas of the device.

2. Corrosive fluxes should not be used to facilitate soldering.

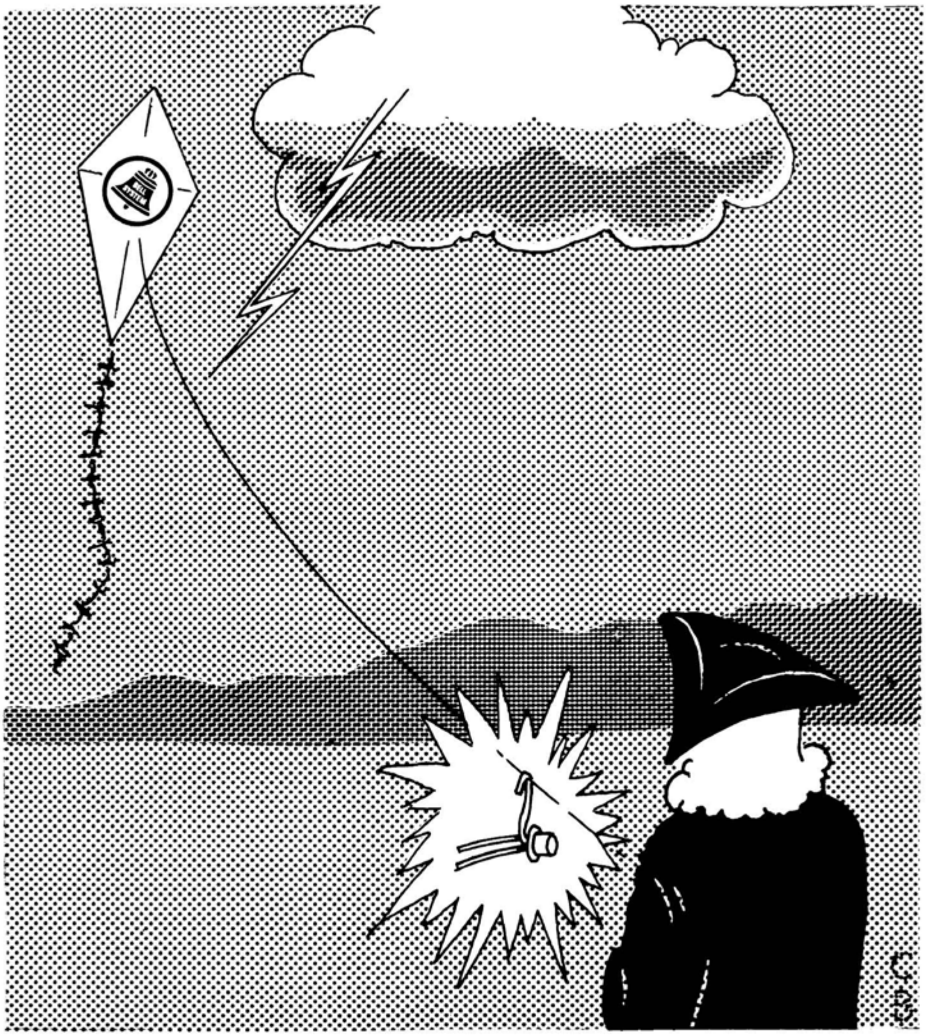
3. Diffused type devices can withstand higher temperatures for longer periods of time than can alloyed types which use lower temperatures in processing. As an example, diffused transistors of the 15- or 16-type families can withstand a 575^{O}F bath for a period of 1 minute when immersed to not more than 1/16 of an inch from the seal. The 12-type germanium alloy transistor should not exceed 460^{O}F in the same bath for more than 30 seconds. In hand soldering, somewhat higher iron tip temperatures can be used if only one lead is heated at a time. For example, with the 12-type germanium transistor the temperature of the iron tip should not exceed 930^{O}F at a minimum distance of 1/16-inch away from the seal for a short duration.

4. Resoldering of thin film circuits should be avoided since local stresses may be developed, resulting in cracked substrates.

5. Any soldering information which may be included in the device data sheets should be followed.

STATIC CHARGES AND TRANSIENTS

A static charge of several thousand volts can easily build up on your body from simply walking about on a nonconductive floor, or moving around in a chair. This is particularly true in low humidity, and when clothing made of wool or certain synthetic fibers, such as nylon, is worn. Ordinarily, this static charge may be high enough to send a damaging pulse through a semiconductor device when it is touched. Before handling ultra-high frequency transistors, milliwatt NPN germanium alloy transistors, and microwave point-contact diodes, be sure to ground static charges by touching some grounded metal object, such as the metal work bench. In extreme cases, sensitive devices may require handling in a completely shorted condition, and operators may require special grounding facilities.

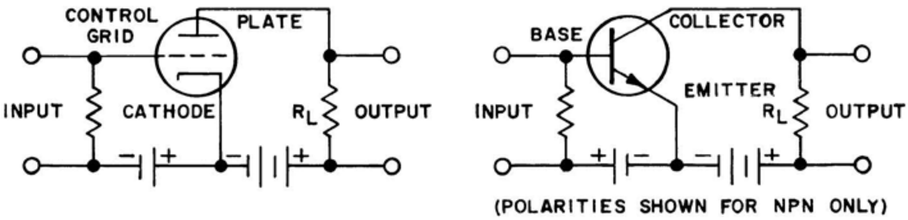


HANDLING

Electric tools, such as screwdrivers and wirewrappers, are frequently used in the assembly of circuit boards containing semiconductor devices. Some devices can be damaged by transients generated by these tools. Air-operated tools are recommended for working on circuits employing ultra-high frequency transistors, milliwatt germanium NPN alloy transistors, microwave point-contact diodes, and epitaxial devices.

BLANK

The long established procedures and equipment for testing electron tube circuits do not directly apply to circuits using semiconductor devices. This is true because parameters are greatly dependent on temperature and strict limits exist on the upper values of applied voltage. If voltage limits are exceeded an abrupt change in impedance may take place which usually results in damage unless the circuits are designed to limit the current.



TUBE-TRANSISTOR ANALOGY

CIRCUIT TESTING

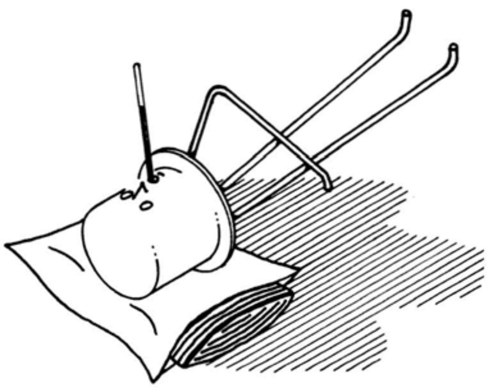
Performance tests on completed circuits must be made in such a way that ratings will not be exceeded for even very short periods of time. Exceeding these ratings may cause a sudden, permanent change of characteristics or may start a long slow change resulting in eventual circuit failure.

Transient energy in the form of voltage spikes or current surges may be generated when sudden changes occur, such as turning a circuit on or off. Similar effects are produced by momentary shorts in live circuits or connection of a low impedance probe for troubleshooting.

These undesirable transients may exceed the maximum ratings of devices in the circuit and cause damage. Caution should be used to prevent or minimize their occurrence.

It is good practice to turn off the power when connecting or removing circuit boards from a test set. In some cases, it may be necessary to short the test set connector terminals in order to discharge the energy stored in wiring and other capacitance in the test set, even though all power supplies are disconnected.

After all necessary connections are made and test set connector short circuits removed, test voltages can be applied in a particular sequence. The BTL circuit design engineer can provide this sequence.



Consideration must be given to ambient temperature when testing solid state circuits, since some semiconductor device parameters can undergo a 2-to-1 change when the temperature is changed as little as 10°C.

Following the operating tests, all voltages should be returned to zero in a proper sequence. In the special case mentioned previously, the test set terminals must be shorted before the circuit under test is removed.

Devices particularly susceptible to test set transients are microwave point-contact diodes, ultra-high frequency transistors, and germanium NPN alloy transistors.

CIRCUIT TROUBLESHOOTING

When it is necessary to troubleshoot and repair an assembled circuit which does not operate properly many approaches can be taken. It is not within the scope of this book to define methods of locating defects, but rather to offer precautionary suggestions which may apply.

"Buzzers" of the electromechanical type, often used as continuity testers, are prolific generators of high-energy transients. Destructive transients may be developed, even though the buzzer battery voltage is much lower than the normal voltage applied to the circuit under test. For this reason, such "buzzers" should never be used when troubleshooting circuits containing semiconductor devices.

Wiring continuity tests can be made safely by use of a selected ohmmeter or electronic buzzer, that is, one that does not exceed the current or voltage ratings of the devices in the circuits being tested.

Typical ohmmeters and a special "Buzzer" developed at Western Electric, Omaha are compared in the following table:

TYPICAL OHMMETER DATA

Description	MAX SHORT CIRCUIT CURRENT (Low Ohm Scale)	MAX OPEN CIRCUIT VOLTAGE (High Ohm Scale)	MAX POWER TO DEVICE UNDER TEST
Omaha "Buzzer" SID 321011	1 MA	0.5 Volts	0.25 MW
Triplett Model 630-L			
X1 and X10	12 MA	0.14 Volts	0.42 MW
X1K and X100K	0.34 MA	34 Volts	0.68 MW
Hewlett-Packard Model 412A	10 MA	1 Volt	2.5 MW
Simpson Model 260	140 MA	7.5 Volts	30 MW
Triplett Model 310	80 MA	16 Volts	30 MW
RCA Voltohmyst Model WV-97A	150 MA	1.5 Volts	60 MW
Weston Analyzer Model 980 Mark II	60 MA	4 Volts	90 MW
Triplett Model 630	350 MA	34 Volts	112 MW

Because of its low voltage, low current and limited power the Omaha "Buzzer" is recommended for continuity testing of any circuits containing semiconductor devices. It is always good practice to remove all power to a circuit when an ohmmeter is used. Even though power is removed transients can result from connecting or disconnecting an ohmmeter across a transformer winding or other inductive element. Damage to a semiconductor device in an adjacent circuit may result.

Troubleshooting by bias measurement or signal tracing is, of necessity, performed with power on. Connecting or disconnecting test probes may cause damage to a semiconductor device by transients because of the effects of their low impedance or high input capacitance. Probe input capacitances may become charged at one point in the live circuit and then, at the next point of application, discharge destructive energy through a semiconductor device. The practice of using high impedance probes and, if necessary, shorting between readings will eliminate this problem.

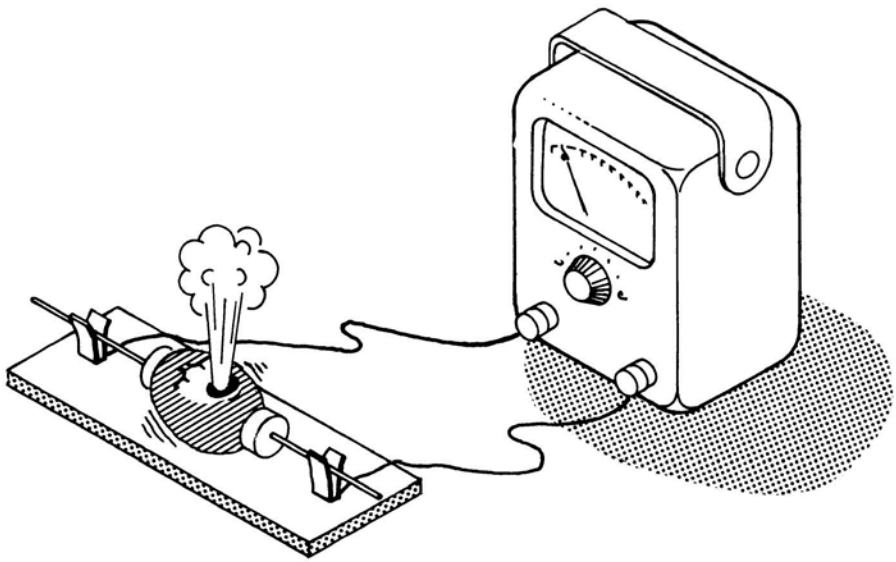
Improper grounding may cause leakage currents from ac-line-operated test equipment, which will result in damage to devices in the circuit under test.

High voltage static charges which build up on clothing, particularly in low-humidity environments, may be injurious to some low-power semiconductor devices if discharged through them. This can be easily avoided by touching a grounded metal object before handling a semiconductor circuit. Use of conductive flooring and the wearing of suitable clothing and shoes may also be employed to prevent the build-up of static charges.

DEVICE TESTING

Transistors and diodes can be tested as individual units by removal from the system or while wired into a circuit. Precautions should be followed to avoid exceeding the device ratings as described in the sections on Circuit Testing and Troubleshooting.

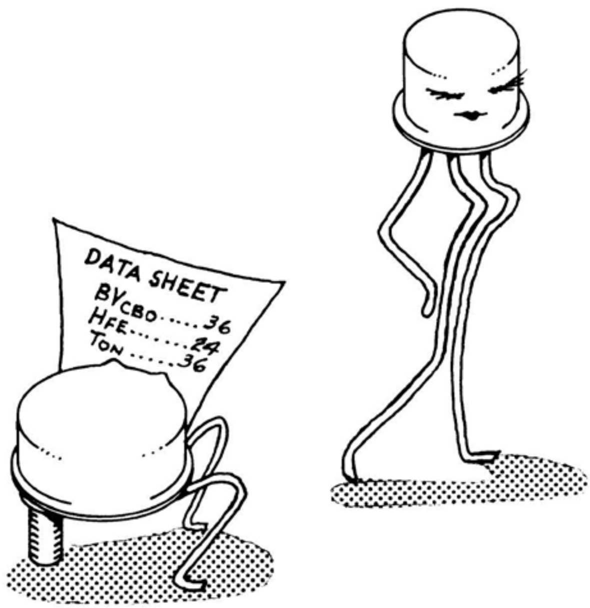
Several general-purpose transistor and diode testers are available commercially which will measure several of the functional parameters. Tests of dc parameters such as leakage current, breakdown voltage and current gain (of transistors) will indicate the normal type of failures such as opens, shorts or appreciable degradation since it was thoroughly tested by the manufacturer. (The Hickok Model 870 is a typical example of a commercial tester.)



In some instances an ohmmeter may be used to indicate opens or shorts. Any tester selected should be checked by the user to assure that it does not apply voltages or currents exceeding the ratings of the device being tested.

A common method of making a quick check of a semiconductor device or thin film circuit believed to be dynamically defective is to insert it into a circuit or system known to be in working order. All power to the circuit should be removed before inserting the "doubtful" device to reduce transients. In some circuits it may also be necessary to discharge circuit capacitances in order to eliminate harmful transients before inserting devices. A device known to be good should never be placed into a defective circuit since the device itself may be damaged. Units suspected of dynamic failure should be brought to the attention of the device manufacturer.

When testing a semiconductor wired into a circuit, refer to the precautions listed for Circuit Testing and Troubleshooting. There are several commercial "in-circuit" testers available, (such as the Hickok Model 890) which can make limited checks without removing a device soldered into the circuit.



Some device parameters are extremely dependent upon the temperature or bias conditions. Leakage currents may double when the temperature is increased about 10°C. Transistor current gain (common emitter) may vary more than 2-to-1, as the emitter current is varied within the ratings of the device. Consult the device data sheets for proper temperature and bias conditions when testing to specification limits.

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Failure Classification

INTRODUCTION

Complex electronic system reliability is determined by the reliabilities of the various devices and parts used. Intrinsic device reliability is obtained through good design, processing and controls. Essential to this stability is purity to an atomic level and an encapsulation or package to hold the environment of the active element constant with time.

The user can appreciably lower the intrinsic reliability through excessive exposure to thermal, electrical or mechanical conditions. Disastrous results may be caused by test set transients, improper switching sequences, inductive surges, power line leakage currents, static discharges, capacitance discharges, and troubleshooting equipment and techniques, by overloading the device junction for a brief instant. The effect of energy concentrated in a small volume is a rapid rising temperature (a hot spot), which alloys through causing an electrical short. On occasion the very fine connecting wires are vaporized causing an open.

The integrity of the seal and the can may be degraded by shock or stress due to mishandling. A lead bent close to a very thin metal-to-glass seal, or shock transmitted by lead clipping or pulling, may initiate a slow leak and destroy the balance of gases, and purity levels. A relatively slow leak will cause a device to show up in time as a field failure.

CATEGORIES

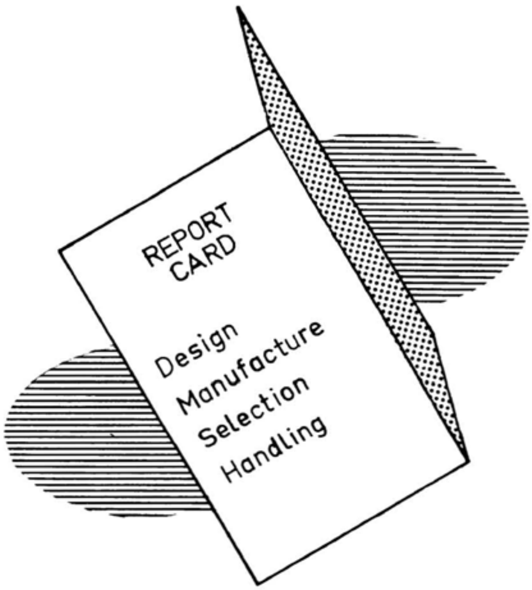
Failures, in general, are classified into four categories:

1. Device Design - Failure to meet reliability <u>design</u> objectives.

2. Device Manufacture - Improper device manufacturing techniques and workmanship.

3. System Design - Incompatability between device selection and equipment specification.

4. System Manufacture or User - Improper techniques in handling and assembling devices into circuits and systems.



It is important and economical to establish a system to recognize the symptoms and understand the causes of failure so as to assign the failure to the proper category when it occurs in a system or subassembly. By proper analyses at the location of the system manufacturer or user (distributing house), made by an expert who is properly trained for the task, many of the failures can be effectively analyzed, and corrective action taken in the shortest possible time. Experience has shown that during the early system testing period of a new device most failures have resulted from mishandling and improper testing procedures. Since all failures will occur in the system manufacturing or user area, the following steps are recommended:

SYSTEM MANUFACTURE OF USER AREA

a. Each using area should establish a failure analysis engineer who has been properly trained for this task at Allentown and Reading so that maximum use can be made of the analysis data. He should be thoroughly familiar with device construction, electrical parameters, testing, handling, and known modes of failure. This specialist should perform only the necessary analyses to determine whether the failure was the result of mishandling, testing, and other user operations or the result of a device anomaly. He should also fill in the failure reports, and keep a record of all failures from all assembly lines so as to detect trends and patterns and notify the appropriate "project engineer" (the engineer responsible for the equipment using the solid state devices). Failure analysis reports should be distributed as follows:

   1. Reports of failures resulting from mishandling, testing, or other system manufacturing operations should be forwarded to the proper "project engineer" with complete information of the analysis. A copy of this report should also be sent to the Reliability Engineering Organization at the device manufacturing location especially if there are a significant number of such failures.

   2. Reports of failures resulting from other causes and the devices should be forwarded to the Reliability Engineering Organization at the device manufacturing location for further analyses and proper action.

b. It should be the responsibility of the project engineer to institute a failure report for each semiconductor device failure. This report should contain complete information, such as the conditions that existed at the time of failure, other devices that failed at the same time, date code, location of device manufacture, etc. The device and the failure report should then be forwarded to the failure analysis engineer. The "project engineer" should also be responsible for taking corrective action where necessary as dictated by the information fed back by the failure analysis reports.

RECOMMENDED AIDS FOR THE FAILURE ANALYSIS ENGINEER

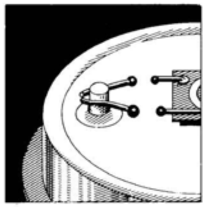
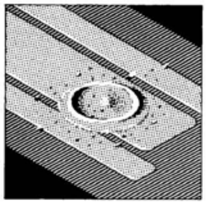
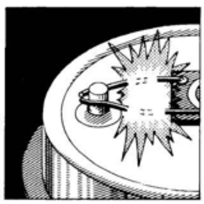
a. Tektronix Type 575 Transistor Curve Tracer or equivalent for electrical analysis.

b. De-canning Tool for Autopsy C-694276 (Allentown drawing) or C-732259 and C-732273 (Reading drawings) for opening enclosures.

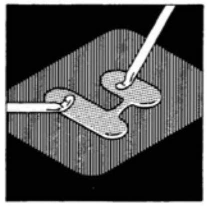
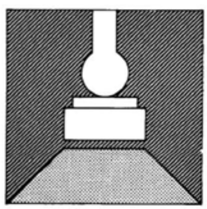
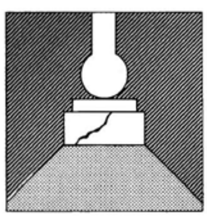
c. Microscope Holding Fixture C-732134 (Reading drawing) for ease of visual inspection.

d. Chart of possible symptoms and causes of semiconductor device failure. (The symptoms are shown for particular geometries, however, they apply equally well to the various geometries which are used for solid state devices.)

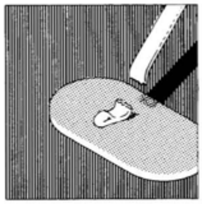
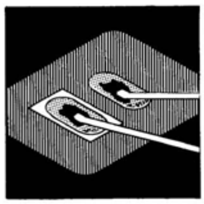
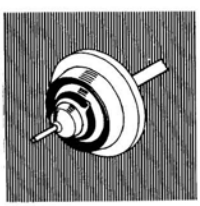
FAILURE CLASSIFICATION

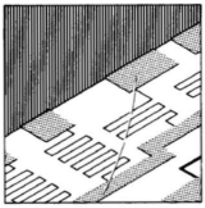
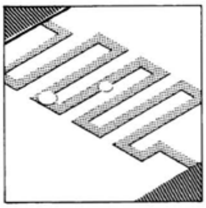
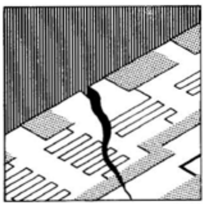
SYMPTOMS		POSSIBLE CAUSES OF FAILURE
Balls on ends of open wires		Excessive current or voltage
Fused spot on wafer		Excessive current or voltage
Vaporized wire		Excessive current or voltage
Discoloration of wire or wafer and device shorted		Excessive current or voltage

SOLID STATE DEVICES

SYMPTOMS		POSSIBLE CAUSES OF FAILURE
Fused streak across wafer or spike between stripes		High voltage or static discharge
Wire lifted from stripe		Poor wire bond - Excessive mechanical shock
Wafer off header		Poor wafer bond - Excessive mechanical shock
Cracked wafer		Severe shock

FAILURE CLASSIFICATION

SYMPTOMS		POSSIBLE CAUSES OF FAILURE
Fractured wire at bond or weld		Poor bond or weld - Excessive vibration
Fractured end of wire at Al stripe. Purple color present near wire		Migration of gold from wire to Al stripe sometime called "purple plague"
No observable defect, but device is shorted internally		Static discharge, high voltage pulse, or contamination
Particle or thread like foreign material across junction area		Physical defects due to poor assembly practices

SYMPTOMS		POSSIBLE CAUSES OF FAILURE
Open or high resistance		Scratch due to rough handling
Open or high resistance		"Pinhole" due to manufacturing defect
Open or high resistance. Broken substrate		Cracked substrate due to shock

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TRANSISTORS

Code	Description	Package	Status	Power (Watts) @ 25 C	BV_{CBO} BV_{CES} ◆ (Min.)	I_{CBO} (μAdc) (Max.)	BV_{EBO} (Min.)	$V_{CE}(sus)$ BV_{CEV} ◆ (Min)	$-h_{fb}$ $-h_{FB}$ ◆ (Min.)	$t_d + t_r$ (nsec) (Max.)	$t_s + t_f$ (nsec) (Max.)	f_T (Med) f_T (Min) ◆ (Mc)
7A	Alloy Ge P-N-P	P-6	A&M	0.25	40	10	20	30 ◆				2.6
7B	Alloy Ge P-N-P	P-6	A&M	0.25	40	10	20	10 ◆	0.980			14.0
8B	Alloy Ge N-P-N	P-6	P	0.25	30	15	30	30 ◆	0.968 ◆			
8C	Alloy Ge N-P-N	P-6	R	0.25	37	15	30	37 ◆	0.968 ◆			
9A	Alloy Ge P-N-P	P-9	P	30.0	60	300	50	60 ◆	0.950			
9B	Alloy Ge P-N-P	P-9	R	2.80	40	20			0.980			
9D	Alloy Ge P-N-P	P-9	P	2.80	40	20			0.970			
12A	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	30 ◆	0.930 ◆			1.2
12B	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	10 ◆	0.980			4.2
12D	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	35 ◆	0.950 ◆			2.1
12E	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	35 ◆	0.950 ◆			
12F	Alloy Ge P-N-P	P-6	P	0.25	45	10	20	45 ◆	0.940 ◆			2.0
12G	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	25 ◆	0.980 ◆			3.3
12H	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	40 ◆	0.970 ◆			2.4
12J	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	25 ◆	0.980			
12K	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	10 ◆	0.980			4.2
12L	Alloy Ge P-N-P	P-6	R	0.25	40	10	20	10 ◆	0.980			4.2
12M	Alloy Ge P-N-P	P-6	P	0.25	40	10	20	10 ◆	0.980			

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ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

Code	Description	Package	Status	Power (Watts) @ 25 C	BV_{CBO} BV_{CES} ♦ (Min.)	I_{CBO} (μAdc) (Max.)	BV_{EBO} (Min.)	$V_{CE}(sus)$ BV_{CEV} ♦ (Min)	$-h_{fb}$ $-h_{FB}$ ♦ (Min.)	$t_d + t_r$ (nsec) (Max.)	$t_s + t_f$ (nsec) (Max.)	f_T (Med) f_T (Min) ♦ (Mc)
12N	Alloy Ge P-N-P	P-6	P	0.25	65	10	20	65 ♦	0.960 ♦			
15A	Diff. Ge P-N-P	P-8	P	0.25	30	6.0	0.8	15 *	†15-330			400 ♦
15B	Diff. Ge P-N-P	P-8	P	Same as 15A except $V_{CE}(sat)$ = 1.5 Vdc maximum								
15C	Diff. Ge P-N-P	P-8	P	0.25	30	6.0	0.8	15 *	†30-200			400 ♦
15D	Diff. Ge P-N-P	P-8	R	Same as 15C except NF = 31.0 db max. at f = 1 kc; $V_{CE}(sat)$ = 3.0 Vdc Max.								
16A	Diff. Si N-P-N	P-1	A&M	0.40	60 ♦	0.1	7.0	22	0.970			300 ♦
16B	Diff. Si N-P-N	P-1	A&M	0.40	90 ♦	0.1	7.0	35	0.972			300 ♦
16C	Diff. Si N-P-N	P-1	P	0.40	35 ♦	0.1	6.0	12	0.978 ♦		200 **	220 ♦
16D	Diff. Si N-P-N	P-1	A&M	0.40	60 ♦	0.1	7.0	28	0.980			350 ♦
16E	Diff. Si N-P-N	P-1	A&M	0.40	60 ♦	0.1	7.0		0.970 ♦	Sum	<100	300 ♦
16F	Si Planar N-P-N	P-1	P	0.40	60 ♦	0.03	6.0	22	0.950 ♦			300
16G††	Si Planar N-P-N	P-1	P	0.40	60 ♦	0.03	6.0	28	0.960 ♦			300
16H	Si Planar N-P-N	P-1	P	Same as 16F with 5 db NF								
16J††	Si Planar N-P-N	P-1	P	0.40	65 ♦	0.1	6.0	24	0.976		150 **	300
16K	Si Planar N-P-N	P-1	P	0.40	110 ♦	0.03	6.0	35	0.968			300
16L	Si Planar N-P-N	P-1	P	0.40	90 ♦	0.03	6.0	35	0.972			220
17A	Alloy Ge P-N-P	P-1	R	0.24	20	1.3	10	20 ♦	0.980			
17B	Alloy Ge P-N-P	P-1	R	0.24	20	2.9	20	15 ♦	0.952			
17C	Alloy Ge P-N-P	P-1	R	0.24	38	2.0	20	36 ♦	† 43			

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TRANSISTORS

Code	Description	Package	Status	Power (Watts) @ 25 C	BV_{CBO} BV_{CES} ♦ (Min.)	I_{CBO} (μAdc) (Max.)	BV_{EBO} (Min.)	V_{CE}(sus) BV_{CEV} ♦ (Min)	$-h_{fb}$ $-h_{FB}$ ♦ (Min.)	$t_d + t_r$ (nsec) (Max.)	$t_s + t_f$ (nsec) (Max.)	f_T (Med) f_T (Min) ♦ (Mc)
18A	Two 16A's	P-7	A&M	The product of the two h_{fe}'s is 3200 to 14,000								
18B	Two 16A's	P-7	A&M	Same as 18A except one of the two transistors has a NF = 6 db max.								
18C	Two 16F's	P-7	R	The product of the two h_{fe}'s is 3200 to 14000								
19A	Three 16A's	P-7	A&M	The product of the three h_{fe}'s is 18 x 10^4 to 18 x 10^5								
20B	Diff. Si N-P-N	P-73	A&M	1.50	60 ♦	1.0	7.0	30	0.962			180 ♦
20C	Diff. Si N-P-N	P-73	A&M	1.50	60 ♦	1.0	7.0	22	0.952			180 ♦
20D	Diff. Si N-P-N	P-73	A&M	1.50	75 ♦	1.0	7.0	50	0.952 ♦	150	350	140 ♦
20E	Diff. Si N-P-N	P-73	A&M	1.50	92 ♦	1.0	7.0	22	0.952			180 ♦
20F	Diff. Si N-P-N	P-73	A&M	1.50	75 ♦	1.0	6.0	30	0.955 ♦	80	150	200 ♦
20G	Diff. Si N-P-N	P-73	A&M	1.50	75 ♦	1.0	6.0	30	0.952			110 ♦
20H	Diff. Si N-P-N	P-73	A&M	1.50	75 ♦	1.0	6.0	32	0.952 ♦	100	600	110 ♦
20J	Si Planar N-P-N	P-67	P	1.50	55 ♦	0.5	6.0	30	† 27			180
20K	Si Planar N-P-N	P-67	P	1.50	60 ♦	0.5	6.0	22	† 22			180
20M	Si Planar N-P-N	P-67	P	1.50	92 ♦	0.5	6.0	22	† 22			180
20N††	Si Planar N-P-N	P-67	P	1.50	75 ♦	0.5	6.0	30	★ 25	90	150	180
20P	Si Planar N-P-N	P-67	P	1.50	75 ♦	0.5	6.0	30	† 22			110
21A	Diff. Si N-P-N	P-71	A&M	0.40	60 ♦	0.1	7.0	22	0.944 ♦	85	40	200 ♦

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$^*BV_{CEO}$ $^{**}t_s$ † h_{fe} †† Epitaxial ★ h_{FE}

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TRANSISTORS

Code	Description	Package	Status	Power (Watts) @ 25 C	BV_{CBO} BV_{CES}♦ (Min.)	I_{CBO} (μAdc) (Max.)	BV_{EBO} (Min.)	V_{CE}(sus) BV_{CEV} ♦ (Min)	$-h_{fb}$ $-h_{FB}$ ♦ (Min.)	$t_d + t_r$ (nsec) (Max.)	$t_s + t_f$ (nsec) (Max.)	f_T (Med) f_T (Min) ♦ (Mc)
21B	Diff. Si N-P-N	P-71	A&M	0.40	60 ♦	0.1	7.0	18	0.970 ♦	85	40	200 ♦
21C	Diff. Si N-P-N	P-71	A&M	0.40	60 ♦	0.1	7.0	22	0.970 ♦	85	40	200 ♦
21D	Diff. Si N-P-N	P-71	A&M	0.40	60 ♦	0.1	7.0	22	0.970			290 ♦
21F	Si Planar N-P-N	P-71	R	0.40	60	0.03	6.0	22	★ 27	85	40	
21G	Si Planar N-P-N	P-71	R	0.40	60	0.03	6.0	18	★42-184	85	40	
21H	Si Planar N-P-N	P-71	R	0.40	60	0.03	6.0	22	★ 31	85	40	
21J	Si Planar N-P-N	P-71	R	0.40	60	0.03	6.0	22	†44-184			
21K	Si Planar N-P-N	P-71	R	0.40	65	0.1	6.0	24	★ 40	**150		
22A	Two 16A's	P-1	A&M		V_{BE} Difference between the two is 5mVdc max. at T = 40 C							
22B	Two 16F's	P-1	P	Matched for V_{BE} and h_{FE}								
22C	Two 16A's	P-1	A&M		Noise figure of one of the two is 7 db maximum							
23A	Diff. Si N-P-N	P-69	A&M	0.78	90 ♦	0.1	7.0	35	0.972			220 ♦
23B	Si Planar N-P-N	P-69	P	0.78	90 ♦	0.03	6.0	35	0.972			220
24A	Diff. Si N-P-N	P-14	A&M	0.83	90 ♦	0.1	7.0	35	0.972			220 ♦
24B	Diff. Si N-P-N	P-14	A&M	0.83	60 ♦	0.1	7.0	35	0.975			260 ♦
24C	Si Planar N-P-N	P-14	P	0.83	90 ♦	0.03	6.0	35	0.972			220
24D††	Si Planar N-P-N	P-14	P	0.83	60 ♦	0.03	6.0	35	0.975			260

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TRANSISTORS

Code	Description	Package	Status	Power (Watts) @ 25 C	BV_{CBO} BV_{CES} ♦ (Min.)	I_{CBO} (μAdc) (Max.)	BV_{EBO} (Min.)	V_{CE}(sus) BV_{CEV} ♦ (Min)	$-h_{fb}$ $-h_{FB}$ ♦ (Min.)	$t_d + t_r$ (nsec) (Max.)	$t_s + t_f$ (nsec) (Max.)	f_T (Med) f_T (Min) ♦ (Mc)
25A	Five 16A's	P-1	A&M		Individual NF of two of the five is 7 db maximum							
26A	Diff. Ge P-N-P	P-11A	P	0.10	20	5.0	0.8	10 *	†15-250	(NF=7.5db Max. @ 70Mc)		500 ♦
26B	Diff. Ge P-N-P	P-11A	P	Same as 26A except NF = 6.0 db Max. @ 70 Mc								
28A	Seven 17A's	P-1	R	Two have h_{fe} 50-100; two h_{fe} 80-200; three h_{fe} 50-200								
29A††	Si Planar N-P-N	P-7	P	0.40	35 ♦	0.1	6.0	30	0.968 ♦	75	125	350
30A	Alloy Ge N-P-N	P-13	P	0.40	30	15	30	30 ♦	0.980 ♦			
30B	Alloy Ge N-P-N	P-13	P	0.40	30	15	30	30 ♦	0.980 ♦			
30C	Alloy Ge N-P-N	P-13	P	0.40	30	15	30	35 ♦	0.988 ♦			
31A	Alloy Ge P-N-P	P-13	P	0.40	40	10	40	40 ♦	0.980 ♦			
31B	Alloy Ge P-N-P	P-13	P	0.40	40	10	40	35 ♦	0.980 ♦			
31C	Alloy Ge P-N-P	P-13	P	0.40	40	10	40	25 ♦	0.988 ♦			
31D	Alloy Ge P-N-P	P-13	P	0.40	40	10	40	40 ♦	0.980 ♦			
32A	Alloy Ge N-P-N	P-9	P	0.95	30	15	30	30 ♦	0.980 ♦			
33A	Two 21B's	P-71	A&M	Each with $t_s + t_f$ = 11-38 nsec and matched within 4.0 nsec								
33B	Two 21G's	P-71	R	Each with $t_s + t_f$ = 11-38 nsec and matched within 4.0 nsec								
35A	Alloy Ge P-N-P	P-6(2)	R	Matched for minimum carrier leak								

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⊕ I_{CES} = 0.06 μAdc **NF = 3.3 db Max. @ 70 Mc *** NF = 4.0 db Max. @ 70 Mc
✚ Dual transistor (two wafers in same enclosure) each exhibiting the electrical characteristics given.

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TRANSISTORS

Code	Description	Package	Status	Power (Watts) @ 25 C	BV_{CBO} BV_{CES} ♦ (Min.)	I_{CBO} (μAdc) (Max.)	BV_{EBO} (Min.)	$V_{CE}(sus)$ BV_{CEV} ♦ (Min)	$-h_{fb}$ $-h_{FB}$ (Min.)	$t_d + t_r$ (nsec) (Max.)	$t_s + t_f$ (nsec) (Max.)	f_T (Med) f_T (Min) ♦ (Mc)
35B	Alloy Ge P-N-P	P-6(2)	R	Same as 35A except carrier leak test omitted and noise test<50 db								
36A	Alloy Ge N-P-N	P-6	A&M	Same as 8B except base lead has compound bend								
37A	Alloy Ge P-N-P	P-16	R	1.0	40	60	40	35 ♦	0.988 ♦			
40A††	Si Planar N-P-N	P-3	P	0.30	25 ♦	0.03	5.0	12	0.968 ♦		15▲	
✚41A††	Si Planar N-P-N	P-4	P	0.40	25 ♦	0.06 ⊕	5.0	12	0.968 ♦		15▲	
42A**	Diff. Ge P-N-P	P-11A	P	0.075	20	5.0	0.4	10 *	★50-200			600 ♦
43A	Alloy Ge P-N-P	P-15	P	0.40	40	10	20	40 ♦	0.970 ♦			2.4
44A††	Si Planar N-P-N	P-1	P	0.20	21 ♦	0.01	4.0	12	†40-300			800 ♦
45A††	Si Planar N-P-N	P-65	P	0.20	21 ♦	0.01	4.0	12	†40-300			800 ♦
45B††	Si Planar N-P-N	P-65	P	0.40	21 ♦	0.02	4.0	12	†40-300			800 ♦
45C††	Si Planar N-P-N	P-65	R	0.80	21 ♦	0.04	4.0	12	†40-300			800 ♦
45D††	Si Planar N-P-N	P-65	P	1.0	21 ♦	0.08	4.0	16	†75-300			900 ♦
45E††	Si Planar N-P-N	P-65	P	0.40	21 ♦	0.02	4.0	12	†75-300			800 ♦
45F††	Si Planar N-P-N	P-65	P	0.80	21 ♦	0.04	4.0	12	†75-300			850

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R = Restricted (Check use with Applications Engineer) $*BV_{CEO}$ $**t_s$ ★ h_{fe} †† Epitaxial †h_{FE} ▲ t_s = 15 nsec
⊕ I_{CES} = 0.06 μAdc **NF = 3.3 db Max. @ 70 Mc *** NF = 4.0 db Max. @ 70 Mc
✚ Dual transistor (two wafers in same enclosure) each exhibiting the electrical characteristics given.

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TRANSISTORS

Code	Description	Package	Status	Power (Watts) @ 25 C	BV_{CBO} BV_{CES}♦ (Min.)	I_{CBO} (μAdc) (Max.)	BV_{EBO} (Min.)	V_{CE}(sus) BV_{CEV}♦ (Min)	$-h_{fb}$ $-h_{FB}$♦ (Min.)	$t_d + t_r$ (nsec) (Max.)	$t_s + t_f$ (nsec) (Max.)	f_T (Med) f_T (Min)♦ (Mc)
***45G††	Si Planar N-P-N	P-65	R	1.0	21 ♦	0.08	4.0	15	†100-300			900 ♦
46A††	Si Planar N-P-N	P-64	P	4.0	35 ♦	1.0	4.0	30	†75-150			700 ♦
46C†† F-56578	Si Planar N-P-N	P-64	P	4.0	35 ♦	1.0	4.0	35	†30-200			650 ♦
46D††	Si Planar N-P-N	P-64	R	4.0	35 ♦	1.0	4.0	35	†50-100			650 ♦
46E††	Si Planar N-P-N	P-64	R	4.0	35 ♦	1.0	4.0	30	†35-75			600 ♦
F-56869††	Si Planar P-N-P	P-1	P	0.36	50 ♦	0.01	5.0	35	†40-250			95 ♦

P = Preferred Note: Power ratings are for free air operation. All electrical values are "Initial Limits"

R = Restricted (Check use with Applications Engineer) *BV_{CEO} **t_s ★h_{fe} †† Epitaxial † h_{FE} ▲t_s = 15 nsec

⊕ I_{CES} = 0.06 μAdc **NF = 3.3 db Max. @ 70 Mc ***NF = 4.0 db Max. @ 70 Mc

✚ Dual transistor (two wafers in same enclosure) each exhibiting the electrical characteristics given.

Care should be taken if any of the breakdown characteristics such as BV_{CEO}, BV_{CES}, BV_{CER} are exceeded. This is particularly true of epitaxial transistors which have low collector body resistance.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

P-N-P-N DEVICES

Code	Description	Package	Status	I (Amps)	BV_F (Min.)*	BV_R (Min.)	I_B for BV_F (mAdc) (Max.)		I_H (mAdc) (Max.)	t_{rr} (nsec) (Max.)
27A	3-Term PNPN Si	P-2	P	0.10	200	200	0.4	10	*10.0	
27B	3-Term PNPN Si	P-2	P	0.10	350	350	1.0	10	*10.0	
27C(F-56522)	3-Term PNPN Si	P-2	R	0.10	200	200	0.165	10	* 3.0	
27D(F-56595)	3-Term PNPN Si	P-2	R	0.10	200	200	.05-.75	10	**10.0	
34A	3-Term PNPN Si	P-70	P	5.0	100	100	5.0	10	* 7.0	
443A	2 Term PNPN Si	P-36	P	0.20	18-24	40			*4-32	100

P = Preferred
R = Restricted (Check use with Applications Engineer)
All Electrical values are Limits Throughout Life.

* For 3 Terminal Devices with R_{BE} = 1000 ohms
** For 3 Terminal Devices with R_{BE} = 0 ohms

RECTIFIERS

Code	Description	Package	Status	Power (Watts) @ 25 C	i_r (surge) (mA pulse) (Max.)	i_f (surge) (A pulse) (Max.)	I_o (Adc) (Max.)	BV (Vdc) (Min.) @	I_R (μAdc)	V_F (Vdc) (Max.) @	I_F (Adc) (Min.)	I_S (μAdc) (Max.) @	V_R (Vdc)
420B	Si Alloy	P-32B	A&M	0.40			.225	200	500	2.0	.010	0.1	160
420D	Si Alloy	P-32B	A&M	0.40			.375	39	500	1.0	.020	0.1	32
420G	Si Alloy	P-32B	A&M	0.40			.300	120	500	2.0	.100	0.1	100
425A	Si Diff	P-31A	P	*10.0		100	10.0	250	10	1.15	10.0	3.0	200
425L	Si Diff	P-31A	P	*10.0		70	7.0	200	10	1.45	7.0	5.0	160
★★425AB	Si Diff	P-31B	P	*10.0		100	10.0	250	10	1.15	10.0	3.0	200
426A	Si Diff	P-30B	P	1.0	3.0	30	1.0	250	10	1.1	1.0	1.0	200
426F	Si Diff	P-30B	P	1.0	4.0	20	1.0	500	10	1.05	1.0	1.0	400
426G	Si Diff	P-30B	R	1.0	2.0	12	.600	1200	25	2.1	0.60	3.0	1000
426H	Si Diff	P-30B	R	1.0	1.5	8.0	.400	1800	25	3.0	0.40	3.0	1500
426J	Si Diff	P-30B	R	1.0	1.0	6.0	.300	2400	25	3.7	0.30	3.0	2000
426K	Si Diff	P-30B	P	1.0	4.0	20	1.0	600	10	1.05	1.0	1.0	500
426L	Si Diff	P-30B	P	1.0	12.5	12	.600	800	10	2.1	0.60	3.0	650
426AF	Si Diff	P-30B	R	1.0		20	1.0	590	10	1.05	1.0	.065	200
435D	Si Diff.	P-29	A&M	0.25		12		120	10	0.90	0.25	0.10	100
440A	Si Diff	P-32B	R	0.75		12	.750	100†	1.0	1.15	0.75	1.0	100
440B	Si Diff	P-32B	R	0.60			.600	250	500	1.1	**0.60	0.1	200
446F	Si Diff	P-34A	P	0.40		3.0	.400	400-950	10	1.0	0.40	2.0	320
446K	Si Diff	P-34A	P	0.40		3.0	.400	600-950	10	1.0	0.40	2.0	480
458A	Si Diff	P-39	P	0.10			.100	75	5.0	1.1	0.40	0.20	40
460A	Si Diff††	P-18	P	0.60			.250	200***	10	1.2	0.250	1.0***	160
460B	Si Diff††	P-18	2Q66★	0.60		2.0*	.400	75	10	1.1	.400	0.20	60
461A	Si Diff††	P-59	P	0.75			.750	200	10	1.2	0.250	1.0***	160
485A	Si Diff	P-72A	10/65★	*10.0		100	10.0	250	10	1.15	10.0	3.0	200

P = Preferred
R = Restricted (Check use with Applications Engineer)
Note: Power ratings are for free air operation
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET

* @ 25°C mounting surface
** Maximum
*** Between adjacent terminals

† P. I. V.
†† 4 Diodes in Bridge Configuration
★ Anticipated availability from WECO
★★ Reverse polarity; case is positive for reverse bias

10 WATT VOLTAGE REGULATORS

Code	Description	Package	Status	BV @ (Vdc)	I_R (mAdc)	V_F @ (Vdc) (Max.)	I_F (Adc) (Min.)	I_S @ (µAdc) (Max.)	V_R (Vdc)	bz @ (ohms) (Max.)	I_R (mAdc)	TCBV (%/°C) (Nom.)
425C	Si Diff.	P-31A	R	22 ± 3.5%	30	1.25	10	3.0	18	12	30	.080
425D	Si Diff.	P-31A	R	18 ± 10%	50	1.25	10	3.0	14.5	4.0	50	.080
425E	Si Diff.	P-31A	P	12 ± 10%	50	1.25	10	1.0	9.5	2.0	50	.080
425F	Si Diff.	P-31A	R	15 ± 10%	50	1.25	10	1.0	12	2.0	50	.070
425G*	Si Diff.	P-31A	P	8.65 ± 5%	10			50	5.0	20	10	.002
425H**	Si Diff.	P-31B	P	22 ± 10%	20	1.25	10	1.0	17.5	12	20	.080
425J	Si Diff.	P-31A	P	22 ± 5%	20	1.25	10	3.0	17.5	12	20	.080
425M	Si Diff.	P-31A	P	8.2 ± 5%	200	1.25	10	10	6.5	3.0	200	.050
425N	Si Diff.	P-31A	P	27 ± 5%	50	1.25	10	4.0	21.5	8.0	50	.085
425P**	Si Diff.	P-31B	R	27 ± 5%	50	1.25	10	50	21.5	8.0	50	.085
425R**	Si Diff.	P-31B	R	18 ± 5%	100	1.25	10	4.0	14.4	5.0	100	.080
425T	Si Diff.	P-31A	P	15 ± 5%	100	1.25	10	4.0	12	4.0	100	.070
425U†	Si Diff.	P-31A	R	12.4 ± 2%	1.0	1.25	10	3.0	9.5	3.0	50	.060
425AA	Si Diff.	P-31A	P	24 ± 5%	50	1.25	10	3.0	20	8.0	50	.085
425AC**	Si Diff.	P-31B	P	8.2 ± 5%	200	1.25	10	10	6.5	3.0	200	.050
485W	Si Diff.	P-72A	R	140 ± 5%	18	1.25	10	3.0	115	100	18	.100
485Y**	Si Diff.	P-72B	R	140 ± 5%	18	1.25	10	3.0	115	100	18	.100

* Intended for low temperature coefficient voltage regulator applications-1 Watt.

** Reverse polarity; case is positive for reverse bias.

† Also BV = 13.2 Vdc max. @ I_R = 200 mAdc.

P = Preferred
R = Restricted (Check use with Applications Engineer)
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

1.0 WATT VOLTAGE REGULATORS

Code	Description	Package	Status	BV (Vdc)	@ I_R (mAdc)	V_F (Vdc) (Max.)	@ I_F (Adc) (Min.)	I_S (µAdc) (Max.)	@ V_R (Vdc)	bz (ohms) (Max.)	@ I_R (mAdc)	TCBV (%/°C) (Nom.)
426E†	Si Diff.	P-30B	R	68 ± 10%	20			3.0	55	30	20	.090
426M	Si Diff.	P-30B	P	22 ± 10%	10	1.0	1.0	1.0	18	30	10	.080
426P	Si Diff.	P-30B	P	12 ± 10%	20			5.0	9.5	10	20	.060
426R	Si Diff.	P-30B	P	18 ± 10%	10	1.0	1.0	1.0	14.5	25	10	.080
426S	Si Diff.	P-30B	P	15 ± 10%	10	1.0	1.0	1.0	12	20	10	.070
426T	Si Diff.	P-30B	P	8.2 ± 10%	20	1.0	1.0	30	5.0	5.0	20	.090
426U††	Si Diff.	P-30B	R	18 ± 10%	10			3.0	14.5	15	10	
426W	Si Diff.	P-30B	P	8.65 ± 5%	10			50	5.0	20	10	.005
426Y†††	Si Diff.	P-30B	R	6.8 ± 10%	20			1.0	6.0	8.0	20	.05
426AB	Si Diff.	P-30B	R	8.65 ± 5%	10			50	5.0	20	10	.003
426AG	Si Diff.	P-30B	P	27 ± 5%	5.0	1.0	1.0	2.0	21.5	50	5.0	.085
426AH	Si Diff.	P-30B	P	75 ± 5%	5.0	1.0	1.0	2.0	60	175	2.0	.090
426AJ	Si Diff.	P-30B	P	15 ± 5%	10	1.0	1.0	2.0	12	17	10	.070
426AK	Si Diff.	P-30B	P	33 ± 5%	10			1.0	26.0	75	10	.070
426AL	Si Diff.	P-30B	P	22 ± 5%	10	1.0	1.0	2.0	17.5	30	10	.080
426AM	Si Diff.	P-30B	R	105 ± 5%	2.0	1.0	1.0	2.0	85.0	350	2.0	.090
470A*	Si Alloy	P-30A	P	4.7 ± 5%	50	1.0	0.5	400	3.0	7.0	50	.030

P = Preferred
R = Restricted (Check use with Applications Engineer)

* Reverse polarity; case is positive for reverse bias

† 6 amp. surge protector
†† 22 amp. surge protector
††† 60 amp. surge protector

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

0.4 WATT VOLTAGE REGULATORS

Code	Description	Package	Status	BV (Vdc)	@ I_R (mAdc)	V_F (Vdc) (Max.)	@ I_F (Adc) (Min.)	I_S (μAdc) (Max.)	@ V_R (Vdc)	bz (ohms) (Max.)	@ I_R (mAdc)	TCBV (%/°C) (Nom.)
420A	Si Alloy	P-32B	A&M	6 ± 10%	10.0	1.0	.030	5.0	3.0	6.5	15.0	.040
420E	Si Alloy	P-32B	A&M	17.5 ± 14%	0.50	1.0	.020	0.1	10	100	10.0	.090
420H	Si Alloy	P-32B	A&M	59 ± 12%	0.50	2.0	.100	0.1	40	160	0.75	.090
420J	Si Alloy	P-32B	A&M	118 ± 8%	0.50	2.0	0.10	0.1	85	400	0.75	.090
420K	Si Alloy	P-32B	A&M	22.5 ± 10%	0.50	2.0	0.20	0.1	16	200	2.5	.080
420M	Si Alloy	P-32B	A&M	8.2 ± 10%	0.50	1.5	0.10	1.0	4.0	27	0.75	.060
420N	Si Alloy	P-32B	A&M	15 ± 10%	0.50	1.0	0.02	0.1	10	100	10	.090
420P	Si Alloy	P-32B	A&M	12 ± 10%	0.50	1.0	0.02	0.1	8.0	100	10	.080
420R	Si Alloy	P-32B	A&M	18 ± 5%	1.0	1.0	0.02	0.1	10	100	10	.090
420S	Si Alloy	P-32B	A&M	8.2 ± 5%	0.5	1.5	0.10	1.0	4.0	27	0.75	.060
420T	Si Alloy	P-32B	A&M	10 ± 10%	0.5	1.0	0.02	0.1	6.0	60	10	.060
446B	Si Diff	P-34A	P	6.2 ± 5%	10.0	1.0	0.40	200	4.5	6.0	10	.035
446C	Si Diff	P-34A	P	8.2 ± 10%	10.0	1.0	0.40	2.0	6.5	7.0	10	.060
446D	Si Diff	P-34A	P	12 ± 10%	10.0	1.0	0.40	1.0	9.5	10	10	.065
446E	Si Diff	P-34A	P	18 ± 5%	5.0	1.0	0.40	1.0	14.5	26	5.0	.085
446G	Si Diff	P-34A	P	27 ± 5%	5.0	1.0	0.40	1.0	21.5	35	5.0	.090

P = Preferred

★Anticipated availability from WECO.

R = Restricted (Check use with Applications Engineer)

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN – USE OFFICIAL DATA SHEET.

0.4 WATT VOLTAGE REGULATORS

Code	Description	Package	Status	BV (Vdc)	@ I_R (mAdc)	V_F (Vdc) (Max.)	@ I_F (Adc) (Min.)	I_S (μAdc) (Max.)	@ V_R (Vdc)	bz (ohms) (Max.)	@ I_R (mAdc)	TCBV (%/°C) (Nom.)
446H	Si Diff	P-34A	P	47 ± 5%	2.0	1.0	0.40	1.0	37.5	210	2.0	.105
446L	Si Diff	P-34A	P	10 ± 5%	10.0	1.0	0.40	2.0	8.0	9.0	10	.070
446M	Si Diff	P-34A	P	15 ± 5%	5.0	1.0	0.40	1.0	12	24	5.0	.075
446N	Si Diff	P-34A	P	22 ± 5%	5.0	1.0	0.40	1.0	17.5	30	5.0	.090
446R	Si Diff	P-34A	P	30 ± 5%	5.0	1.0	0.40	1.0	24	40	5.0	.095
446S	Si Diff	P-34A	P	100 ± 5%	1.0	1.0	0.40	1.0	80	350	1.0	.090
446T	Si Diff	P-34A	P	8.2 ± 5%	10.0	1.0	0.40	2.0	6.5	7.0	10	.065
446U	Si Diff	P-34A	P	62 ± 5%	1.0	1.0	0.40	1.0	49.5	285	1.0	.090
446W	Si Diff	P-34A	P	91 ± 5%	1.0	1.0	0.40	1.0	72.5	345	1.0	.090
446Y	Si Diff	P-34A	P	9.1 ± 5%	10.0	1.0	0.40	2.0	7.2	8.0	10	.065
446AD	Si Diff	P-34A	P	12 ± 5%	10.0	1.0	0.40	1.0	9.5	10	10	.065
448A	Si Alloy	P-34A	P	4.7 ± 10%	20.0	1.0	0.20	250	3.0	18	20	.020
448B	Si Alloy	P-34A	2Q66 ★	4.3 ± 5%	20.0	1.0	0.20	250	3.0	18	20	.020
459E	Si Diff	P-39	3Q66 ★	8.2 ± 5%	10.0	1.0	0.20	2.0	6.5	7.0	10	.060

P = Preferred

★ Anticipated availability from WECO.

R = Restricted (Check use with Applications Engineer)

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

SWITCHING DIODES

Code	Description	Package	Status	Power (Watts) @ 25 C	BV (Min.) @	I_R (μAdc)	V_F (Vdc) (Max.) @	I_F (Adc) (Min.)	I_S (μAdc) (Max.) @	V_R (Vdc)	C † (pf) (Max.)	t_{rr} (μsec) (Max.) @	$I_F = I_R$ (mAdc)
420L	Si Alloy	P-32B	A&M	0.60	80	500	1.1	0.02	10	50.0	100	0.50	10
425K	Si Diff.	P-31A	P	*5.0	100	10	1.3	2.0	3.0	80	800	0.20	30
425L	Si Diff.	P-31A	P	*10.0	200	10	1.45	7.0	5.0	160	400	0.20	100
425S	Si Diff.	P-31A	P	*10.0	250	10	1.15	10.0	3.0	200		3.5-5.5	1500
426L	Si Diff.	P-30B	P	1.0	800	10	2.1	0.60	3.0	650	50	0.1	10
426AC	Si Diff.	P-30B	P	1.0	120	10	**1.35	**1.35	1.0	50	45	0.10	100
426AD	Si Diff.	P-30B	P	1.0	120	10	1.0	1.0	1.0	100	100	0.20	100
432A	Si Diff.	P-35	A&M	0.10	40	5.0	1.0	0.01	0.015	20	4.0	0.004	10
435C	Si Diff.	P-29	A&M	0.25	40	5.0	1.0	0.01	0.015	20	3.5	0.004	10
435E	Si Diff.	P-29	A&M	0.25	40	5.0	0.72	0.002	0.015	20	4.0	0.004	10
446A	Si Diff.	P-34A	P	0.40	120	5.0	1.1	0.40	2.0	100	25	0.05	100
447A	Si Diff.	P-41	A&M	0.10	40	5.0	1.0	0.01	0.025	20	3.5	0.004	10
449A††	Si Diff.	P-34B	P	0.40			2.30	0.0025	2.0	150	15	0.04(Min)	2-10

† @ V_R = 0 Vdc except 449A @ V_F = 1.0 Vdc. & 420L @ V_R = 4.5 Vdc

†† Level Shifter: V_F = 1.53 Vdc Min. @ 70 μAdc. Stored Charge=400 pCb @ i_f=2 mAdc, i_r=10 mAdc.

P = Preferred

R = Restricted (Check use with Applications Engineer)

⊕ Epitaxial

* With Heat Sink

** Peak Pulse

*** Switched Power

NOTE: Power ratings are for free air operation.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

SWITCHING DIODES

Code	Description	Package	Status	Power (Watts) @ 25 C	BV (Min.) @	I_R (μAdc)	V_F (Vdc) (Max.) @	I_F (Adc) (Min.)	I_S (μAdc) (Max.) @	V_R (Vdc)	C † (pf) (Max.)	t_{rr} (μsec) (Max.) @	$I_F = I_R$ (mAdc)
458A	Si Diff.	P-39	P	0.10***	75	5.0	1.10	0.40	0.200	40	30	0.050	100
458B	Si Diff.	P-39	P	0.10***	75	5.0	.71-.84	0.10	0.200	40	30	0.050	100
458C	Si Diff.	P-39	P	0.10***	40	5.0	1.0	0.01	0.015	20	4.0	0.004	10
458D	Si Diff.	P-39	P	0.10***	40	5.0	.62-.72	0.002	0.015	20	4.0	0.004	10
458E ⊕	Si Diff.	P-39	P	0.10***	50	5.0	1.0	0.100	0.050	20	4.0	0.005	10
458F	Si Diff.	P-39	R	0.10***	40	5.0	.30-.37	10^{-6}	0.025	20	5.0	0.005	10

† @ V_R = 0 Vdc except 449A @ V_F = 1.0 Vdc. & 420L @ V_R = 4.5 Vdc

P = Preferred

†† Level Shifter: V_F = 1.53 Vdc Min. @ 70 μAdc. Stored Charge=400 pCb @ i_f=2 mAdc, i_r=10 mAdc.

R = Restricted (Check use with Applications Engineer)

⊕ Epitaxial

* With Heat Sink

** Peak Pulse

*** Switched Power

NOTE: Power ratings are for free air operation.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

GERMANIUM DIODES

Code	Description	Package	Status	Power (Watts) @ 25 C	BV (Vdc) (Min.) @	I_R (mAdc)	I_R (µAdc) (Max.) @	V_R (Vdc)
400A	Pt. Ct.	P-43	P	0.20	60		20/850	5/50
400E	Pt. Ct.	P-43	P	0.20	140		500	50
400F	Pt. Ct.	P-43	P	0.20	60		20/850	5/50
400G	Pt. Ct.	P-43	R	0.20	60		1000	50
400H	Pt. Ct.	P-43	R	0.20	60		20/850	5/50
400J	Pt. Ct.	P-43	P	0.20	140		20/850	5/50
424A	Pt. Ct.	P-32B	R	0.20			3.5/35	5/25
441A		P-40	P	Same as 400A except axial leads				
441F		P-40	P	Same as 400F except axial leads				
441H		P-40	R	Same as 400H except axial leads				
441J		P-40	R	Same as 400J except axial leads				

P = Preferred

R = Restricted (Check use with Applications Engineer)

Note: Power ratings are for free air operation

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

MICROWAVE DIODES

Code	Package	Status	Power (Watts) @ 25 C	BV @ (Vdc) (Min.)	I_R (mAdc)	V_F @ (Vdc) (Max.)	I_F (Adc) (Min.)	I_S I_R ♦ @ (μAdc) (Max.)	V_R (Vdc)	C C_T ♦ (pf) (Max.)	Major Application
404A	P-43	A&M	0.40	~3.0		1.0	.020	150	1.0		High Level Mixer
404B	P-43	A&M	0.40	~3.0				500	2.0		High Level Mixer
404C	P-43	A&M	0.40	~3.0		1.0	.040	500	1.0		High Level Mixer
404D	P-27	A&M	0.40	~3.0		1.0	.040	500	1.0		High Level Mixer
405B	P-25A	R	0.40	~3.0							Detector
405C	P-25A	R	0.02	~3.0							Detector
405D	P-25A	A&M	0.40	~3.0							Detector
405E††	P-25A	R	0.30					100 ♦	1.0		Detector-Monitor
406A	P-26	R	0.02	~3.0							Converter
406B	P-26	R	0.02	~1.0		0.2	.0004	40 ♦	0.2		Converter
431A	P-25B	A&M	0.50	~25		.80	.10	100	7.5		Limiter
444A	P-27	A&M	0.20					100	2.0		Limiter
445A	P-44	A&M	0.15			0.55	0.01	1.0	1.5	1.7	Converter

P = Preferred
R = Restricted (Check use with Applications Engineer)
Note: Power ratings are for free air operation.
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET

* Matched Pair - Unmounted
** Heat Sink at 25 C
*** This rating applies to the pair
† Applies for each diode of the pair
†† Special vswr requirements

MICROWAVE DIODES

Code	Package	Status	Power (Watts) @ 25 C	BV @ (Vdc) (Min.)	I_R (mAdc)	V_F @ (Vdc) (Max.)	I_F (Adc) (Min.)	I_S I_R♦ @ (μAdc) (Max.)	V_R (Vdc)	C C_T♦ (pf) (Max.)	Major Application
471A*	P-23	R	0.1***	†15	0.01	†1.1	.100	†0.1	12	†0.8-1.2 ♦	Transmitter Modulator
472B	P-22	R	0.05	30	0.01	1.1	.100	0.1	24	0.6-0.9 ♦	Harmonic Generator
472C	P-22	R	0.02	20	0.01	1.2	.100	0.1	16	.405-.485 ♦	Parametric Amplifier
472D	P-22	R	0.02	20	0.01	1.2	.100	0.1	16	.455-.535 ♦	Parametric Amplifier
472E	P-22	R	0.02	20	0.01	1.2	.100	0.1	16	.505-.585 ♦	Parametric Amplifier
472F	P-22	R	0.02	20	0.01	1.2	.100	0.1	16	.555-.635 ♦	Parametric Amplifier
473A	P-21	R	2.0**	60	0.01	1.1	.100	1.0	50	3.0-6.0 ♦	Harmonic Generator r
473B	P-21	R	3.0**	80	0.01	1.0	.100	1.0	60	11-19 ♦	Harmonic Generator r
473C	P-21	R	4.0**	70	0.01	1.0	.100	1.0	60	46-68 ♦	Harmonic Generator r
480A	P-38	R	0.03	15	0.01	1.1	.100	0.1	12	0.3-0.6 ♦	70 Mc Gates
488A	P-38	R	0.05	3.0				200 ♦	1.0		I. F. Detector

P = Preferred
R = Restricted (Check use with Applications Engineer)
Note: Power ratings are for free air operation.
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET

* Matched Pair - Unmounted
** Heat Sink at 25 C
*** This rating applies to the pair
† Applies for each diode of the pair
†† Special vswr requirements

MULTIPLE DIODES

Code	Package	Status	Description
100A	P-33	P	0.90 Vdc Max. @ 100 mAdc; 0.20 Vdc Min. @ .01 mAdc in either direction
100D	P-33	R	0.72 Vdc Max. @ 10 mAdc; 0.43 Vdc Min. @ 0.10 mAdc in either direction
100E	P-33	R	Same as 100D except for addition of 50 amp. pulse test
100F	P-33	P	Same as 100A except for addition of 50 amp. pulse test
100G	P-33	P	0.74-0 80 Vdc @ 100 mAdc; 0.43 Vdc Min. @ 0.10 mAdc in either direction
101A	P-33	R	Seven 100A's
103A	P-20	R	Five 100A's molded
104A	P-33	P	Symmetrical germanium fractional voltage limiter, click reducer
401A	P-60	R	Four 400 Types mounted on a standard octal base
403A	P-60	A&M	Four 404 and 405 Types mounted on a standard octal base
403B	P-60	A&M	Two 404 and 405 Types mounted on a standard octal base
403C	P-60	A&M	Two 404 and 405 Types mounted on a standard octal base
407A	P-51	R	Four 400 Types mounted on a plate
407B	P-51	R	Four 400 Types mounted on a plate
407D	P-51	R	Four 400 Types mounted on a plate
407E	P-51	R	Same as 407A except for a mechanical rearrangement
407F	P-51	R	Same as 407B except for a mechanical rearrangement
408A	P-58	R	Six 400 Types mounted on a plate

R = Restricted (Check use with Applications Engineer)   P = Preferred
These diodes have been designed for specific applications. For further information contact the appropriate Applications Engineer.
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

MULTIPLE DIODES

Code	Package	Status	Description
409A	P-74	A&M	Two 404 Types with two leads welded together
410A	P-61	R	Ten 400 Types mounted on a plate with mounting brackets
411A	P-54	R	Two 400 Types mounted on a plate with mounting bracket
413A	P-75	A&M	Twelve 405B's mounted between plates with a mounting bracket
414A	P-76	A&M	Four 405B's mounted between plates with a mounting bracket
415A	P-77	A&M	Four 405B's mounted on a plate and covered by a metal can
416C	P-25A	R	Two 405's with overall NF = 10 db max.
417B	P-79	A&M	Replace with 420G
418A	P-78	A&M	Four 405B's mounted between plates
421A	P-48	R	Two 420 Types mounted on a plate
421C	P-48	R	Two 420 Types mounted on a plate
421D	P-48	R	Two 420 Types mounted on a plate
421E	P-48	R	Two 420 Types mounted on a plate
422B	P-50	R	Four 420 Types mounted on a plate
426N	P-30C	R	A 68V 10% Regulator and 200V Rectifier back-to-back
427A	P-25B	A&M	Two 431A's
433A	P-49	A&M	Two 420 Types in series mounted on a plate

P = Preferred
R= Restricted (Check use with Applications Engineer)
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

These diodes have been designed for specific applications. For further information contact the appropriate Applications Engineer.

MULTIPLE DIODES

Code	Package	Status	Description
433B	P-49	A&M	Two 420 Types in series mounted on a plate
434B	P-47(2)	A&M	Four si. diff. diodes matched for forward impedance
437A	P-42	A&M	Seven 432 Types (unmounted)
438A	P-46(2)	R	Matched for V_F at 20 μAdc, 200 μAdc, and 2 mAdc @ 120 C
439A	P-45(2)	R	Matched for V_F at 20 μAdc, 200 μAdc, and 2 mAdc @ 120 C
442A	P-35	R	Four 432 Types
462A	P-11B	P	Ge. full-wave bridge in single encapsulation
463A	P-55	R	Four 426J's in series - molded
464A	P-56	R	Four 426G's in full-wave bridge - molded
464B	P-56	R	Four 426J's in full-wave bridge - molded
464C	P-56	P	Four 426 Type diodes in full-wave bridge - molded
465A	P-39	R	Seven 458A's matched - unmounted
465B	P-39	P	Seven 458C's matched - unmounted
466A	P-53	P	Four 458A's mounted on board
475A	P-11C	R	Matched pair of diode elements in a single encapsulation
477A	P-31	R	Four 425S's matched for +10% t_{rr} - unmounted
478A	P-57	R	Five 426L's connected in series - molded
478B	P-57	P	Four 426G's connected in series - molded
482A	P-63	P	Eight diode elements with common cathodes in single encapsulation

P = Preferred
R = Restricted (Check use with Applications Engineer)
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

These diodes have been designed for specific applications. For further information contact the appropriate Applications Engineer.

MULTIPLE DIODES

Code	Package	Status	Description
482B	P-63	P	Eight diode elements with common anodes in single encapsulation
483A	P-39	P	Four 458C's matched - unmounted
484A	P-62	R	Two mounted diodes, each in a TO-18 package, matched for forward impedance
484B	P-62	R	Same as 484A, except different forward impedance match
487A	P-68	P	Four 446 Type diodes in bridge configuration - molded
487B	P-68	P	Same as 487A with lower pulse handling capability
489A	P-66	P	Two mounted diodes, each in a TO-18 package, matched for forward impedance
489B	P-66	P	Same as 489A, except different forward impedance match
491A	P-11B	P	Si full-wave bridge in single encapsulation. Polarity ground

P = Preferred
R = Restricted (Check use with Applications Engineer)
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

These diodes have been designed for specific applications. For further information contact the appropriate Applications Engineer.

SPECIAL USE DIODES

Code	Package	Status	Description
426AA	P-30B	R	Variable capacitance diode, C = 900 pf @ V_R 1.0 Vdc
426AE	P-30B		BV = 13.1 - 13.6 @ I_R = 20.0 mAdc
426AN	P-30B	2Q66★	Symmetrical surge protector, ± 18 volt limiter
446J	P-34B	R	Variable capacitance diode, C = 28 pf @ V_R = 4 Vdc
446P	P-34B	R	Variable capacitance diode, C = 28 pf @ V_R = 4 Vdc
446AA	P-34B	R	Variable capacitance diode
446AB	P-34A	R	Same as 446F except i_f (surge) 30 A. for 1 MSec.
446AC	P-34A	R	Same as 446T except 100% life tested for 1000 hours
457A	P-39	R	Variable capacitance diode (High Q), C=16 pf @ V_R 5.0 Vdc
474A	P-12	P	Pin Variolosser Diode in TO-18 type package
476A to AC	P-29	R	Same as 446A to AC except electrically insulated body
479A	P-10	R	Silicon ESBAR diode in three leaded package
481A	P-28	R	One 426J-molded

P = Preferred
R = Restricted (Check use with Applications Engineer)
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

★Anticipated availability from WECO.

Ge BACKWARD DIODES

Code	Package	Status	Power (mW) @ 25 C	I_p (mAdc)	I_p/I_v (Min.)	V_p (mVdc)	C_{Tv} (pf)	R_S (ohms)	Diff. Sens. (mVdc/db) (Min.)	TSF (db/° F) (Max.)	Major Application
486A	P-23	R	0.6	.040-.200	4.0	30-70	.170-.310	6.5-13.5	4.0	9×10^{-4}	R. F. Detector

P - Preferred
R - Restricted (Check use with Applications Engineer)
Note: Power ratings are for free air operation
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN - USE OFFICIAL DATA SHEET.

CERAMIC THIN FILM CIRCUITS

Code	Description and Use*	Package	Status	Tolerance	Noise Index (Max) DB	Delay Time (Nanosec.)
15A	Two 4-Input Gate	P-85	P	±3%	-25	90
15B	One 4-Input Gate	P-85	P	±3%	-25	<45
15C	Two 4-Input Gate - No Power	P-85**	P	±3%	-25	<90
15D	One 4-Input Gate - No Power	P-85**	P	±3%	-25	<45
15E	Four 2-Input Gate	P-84	P	±3%	-25	<180
15F	Three 2-Input Gate	P-84	P	±3%	-25	<135
15G	Two 2-Input Gate	P-84	P	±3%	-25	<90
15H	One 2-Input Gate	P-84	P	±3%	-25	<45
15J	Four 2-Input Gate - No Power	P-84**	P	±3%	-25	<180
15K	Three 2-Input Gate - No Power	P-84**	P	±3%	-25	<135
15L	Two 2-Input Gate - No Power	P-84**	P	±3%	-25	<90
15M	Emitter Follower	P-88	P	±3%	-25	<10
15N	Emitter Follower	P-88	P	±3%	-25	<10
15P	Emitter Follower	P-88	P	±3%	-25	<10
15R	High Fan Out 4-Input Gate	P-86	R	±3%	-25	<50
15S	High Fan Out 2-Input Gate	P-86	R	±3%	-25	<50
15T	Two 4-Input IFO Gate	P-85	P	±3%	-25	<45
15U	One 4-Input IFO Gate	P-85	P	±3%	-25	<45
15W	Two 2-Input IFO Gate	P-85	P	±3%	-25	<45
15AA	High Fan Out Gate	P-87	P	±3%	-25	<45
16A	Time Division Switch	P-81	P	±3%	-25	

*Refer to package number for electrical schematic.

**Electrical schematic same as power types except 750 ohm resistors omitted.

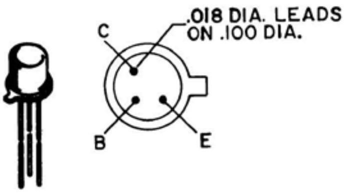
CERAMIC THIN FILM CIRCUITS

Code	Description and Use*	Package	Status	Tolerance	Noise Index (Max) DB	Delay Time (Nanosec.)
16B	Time Division Switch		P	±3%	25	
16C	Time Division Switch		P	±3%	25	
16D	Time Division Switch		P	±3%	25	
16E	Time Division Switch		P	±3%	25	
16F	Time Division Switch		P	±3%	25	
16G	Time Division Switch		P	±3%	25	
17A	One Input TRL Gate	P-90		+3% -2%	25	
17B	Two Input TRL Gate	P-90		+3% -2%	25	
17C	Three Input TRL Gate	P-90		+3% -2%	25	
18A	Four Input TRL Gate	P-92		+3% -2%	25	
18B	Five Input TRL Gate	P-92		+3% -2%	25	
18C	Six Input TRL Gate	P-92		+3% -2%	25	
19A	Triple One-Input Gate	P-91		+3% -2%	25	
20A	Triple Two-Input Gate	P-91		+3% -2%	25	
21A	Triple Two-Input Gate w/Base Leads		P	+3% -2%	25	
23A	Binary Counter & Shift Register	P-80	P	±3%	25	<30
AL1	Line Circuit	P-93		+3% -2%	25	

*Refer to package number for electrical schematic.

GLASS THIN FILM CIRCUITS

Code	Description	Package	Status	Tolerance	Use
N1	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N2	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N3	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N4	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N5	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N6	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N7	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N8	Thin Film Circuit Pack	P-82	P	±3%	TRL Gate
N9	Thin Film Circuit Pack	P-83	P	±3%	TRL Gate
N10	Thin Film Circuit Pack	P-83	P	±3%	TRL Gate
N11	Thin Film Circuit Pack	P-83	P	±3%	TRL Gate



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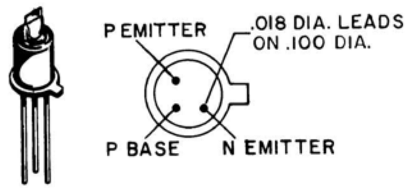

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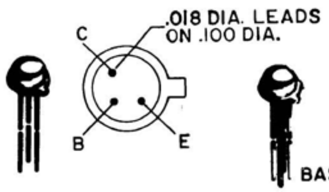

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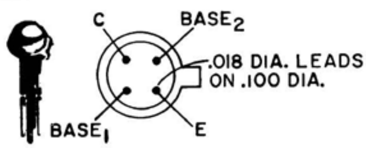

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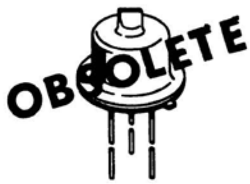

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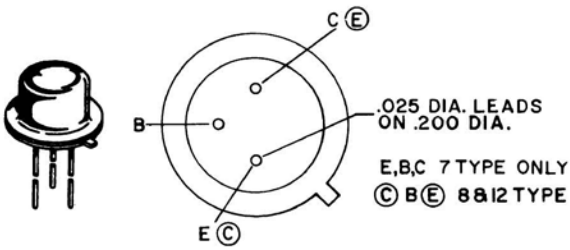

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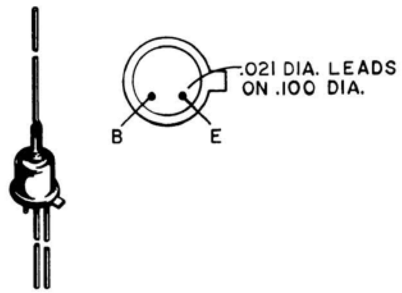
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ON .100 DIA.
B
E

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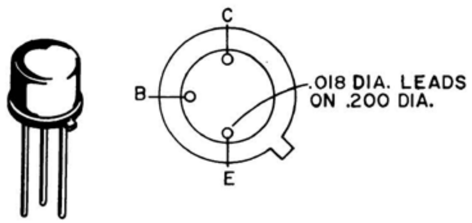
C
B
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E

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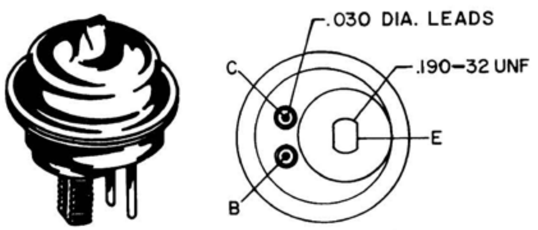
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C
.190-32 UNF
E
B

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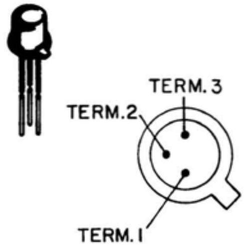

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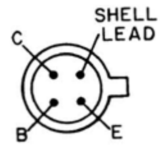

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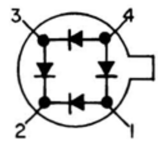

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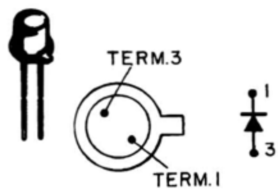

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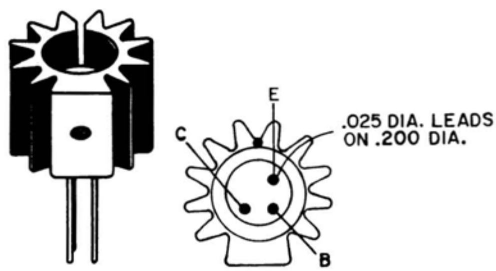

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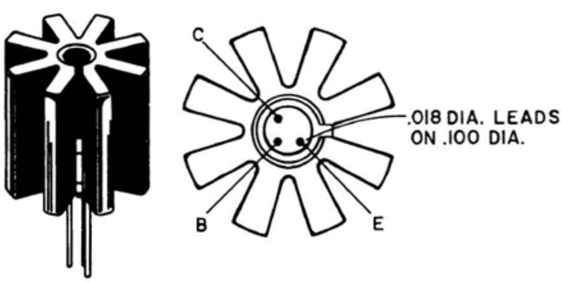

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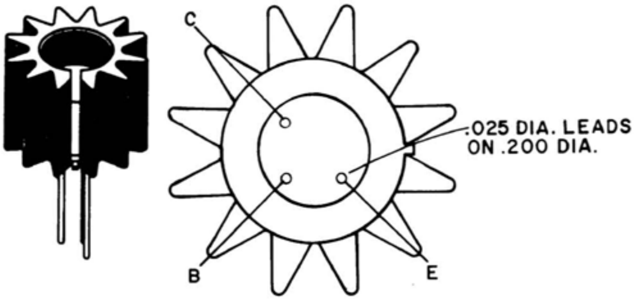

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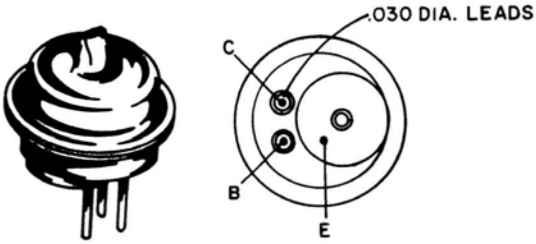

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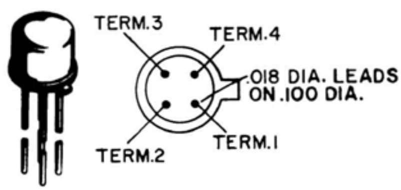

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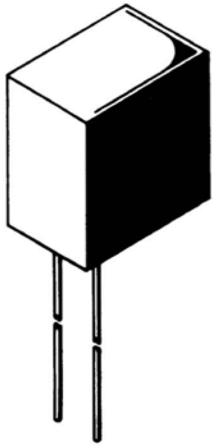

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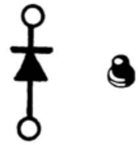

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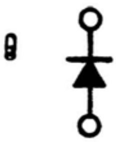

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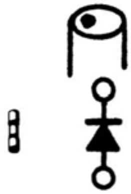

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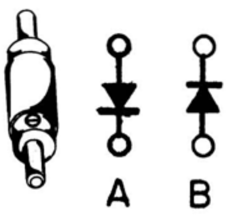

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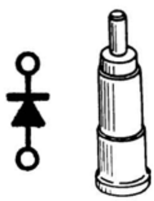

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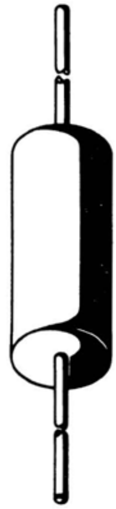

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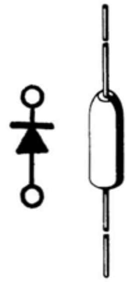

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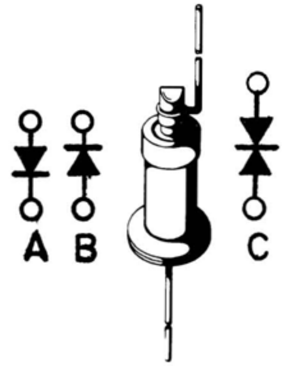

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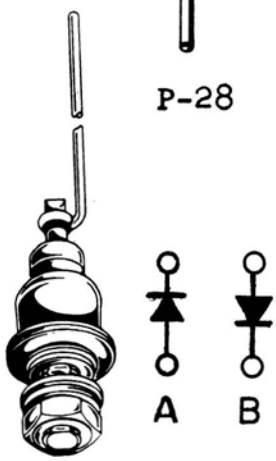

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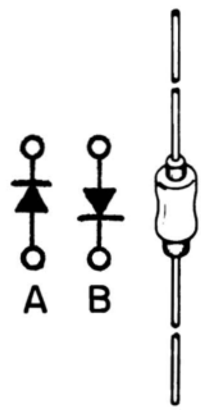

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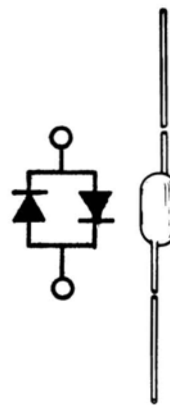

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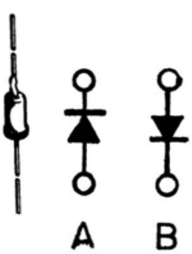

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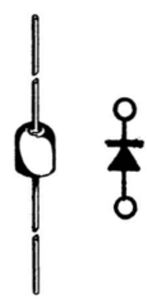

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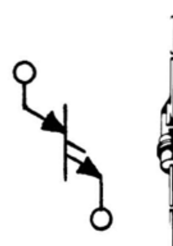

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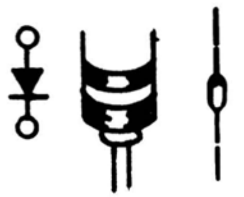

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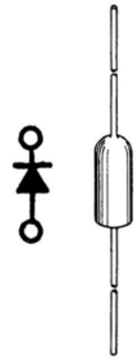

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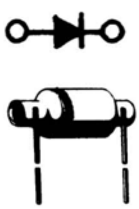

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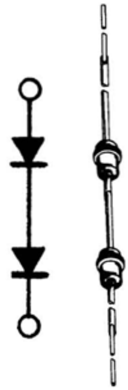

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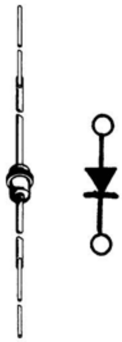

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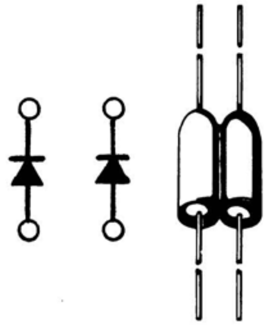

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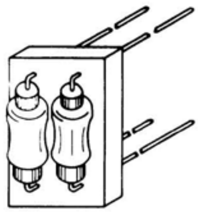

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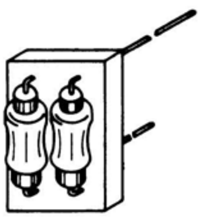

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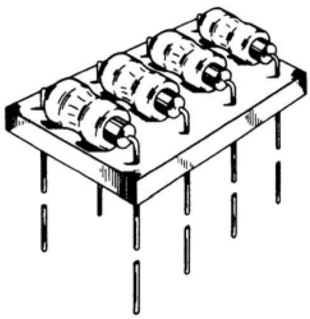

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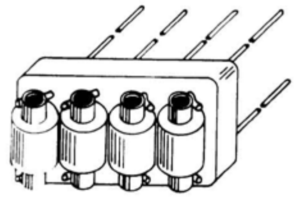

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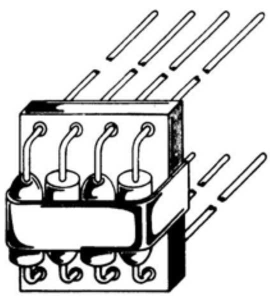

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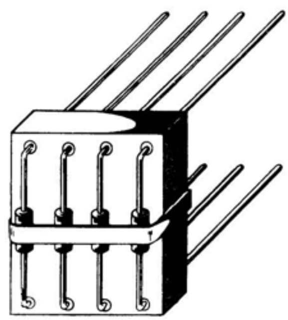

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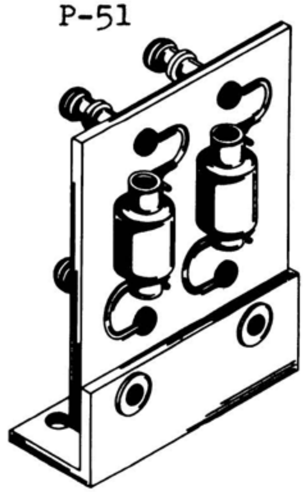

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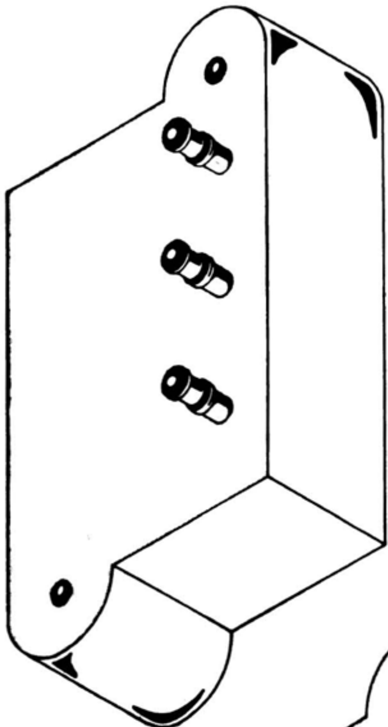

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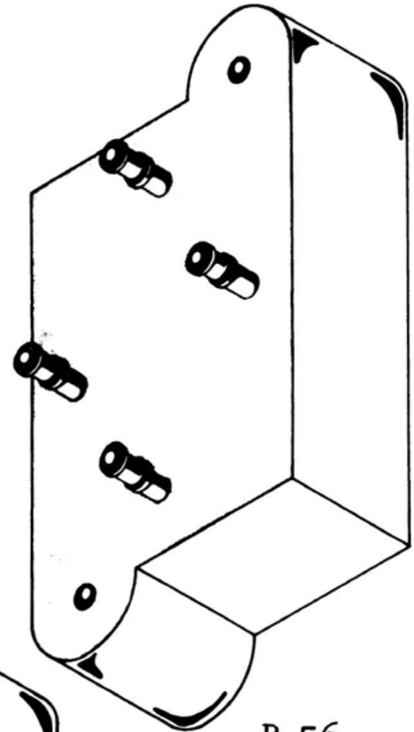

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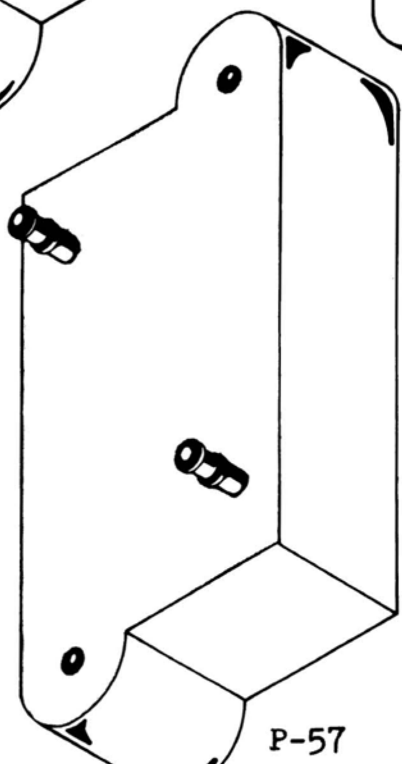

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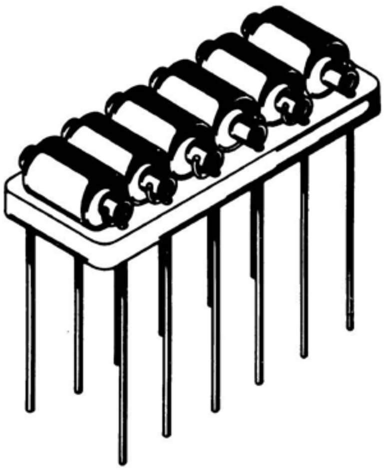

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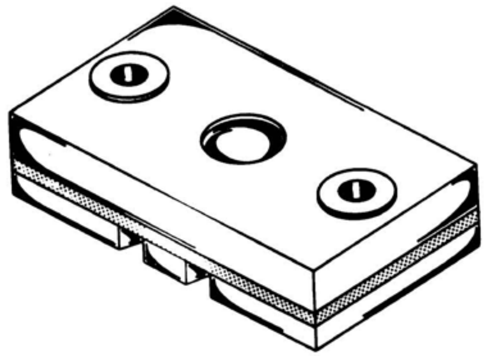

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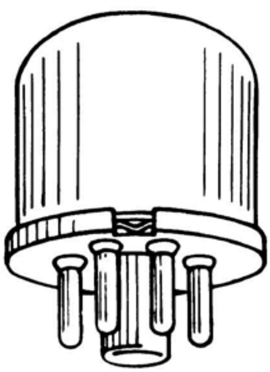

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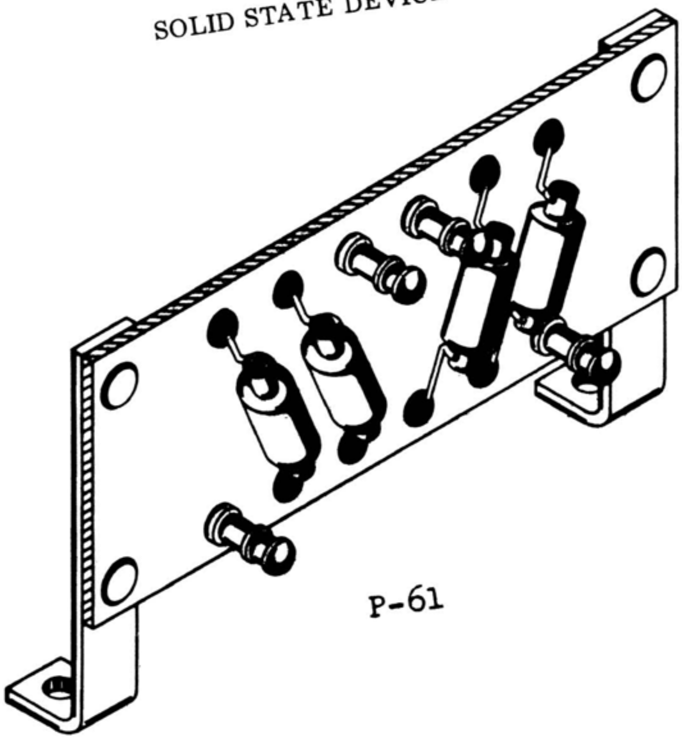

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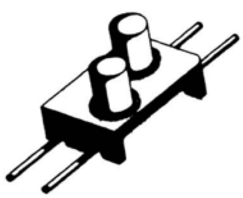

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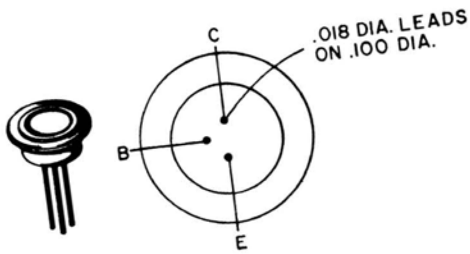

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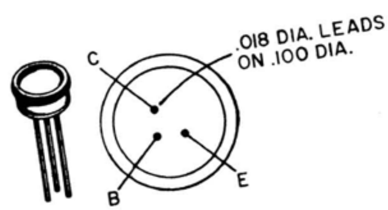

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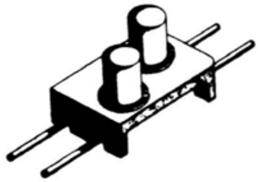

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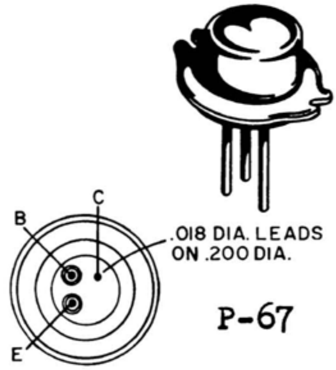

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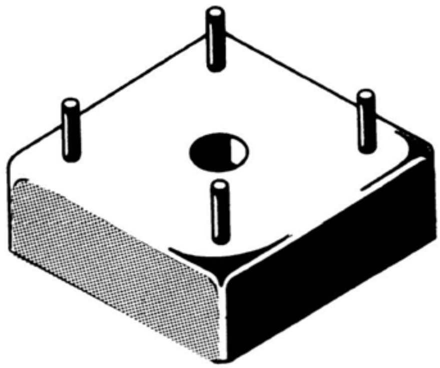

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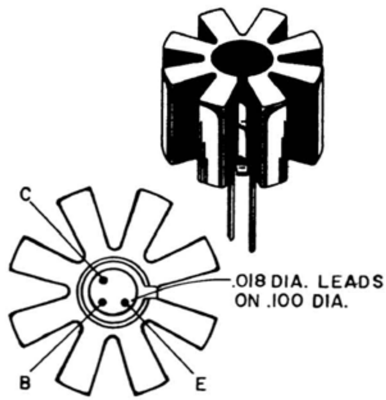

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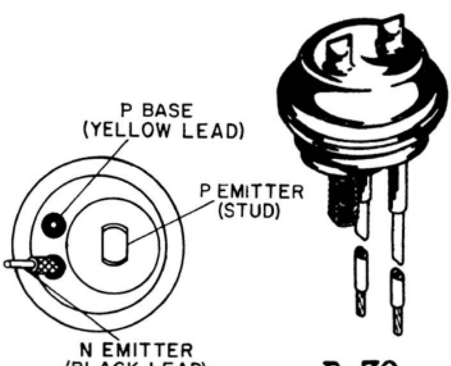

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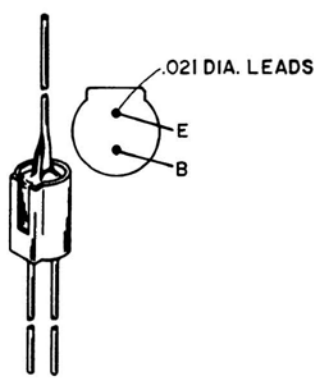

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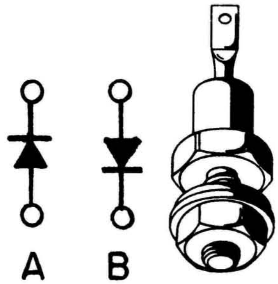

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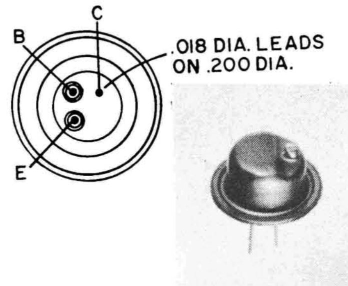

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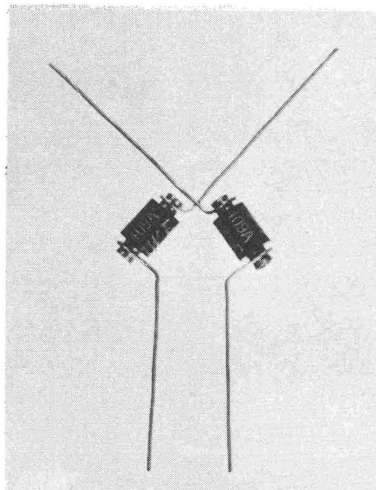

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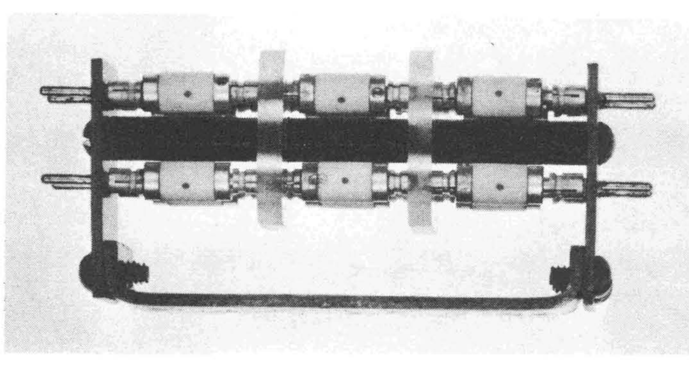

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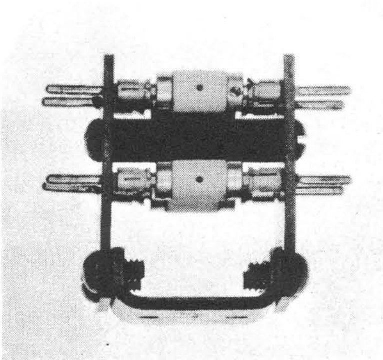

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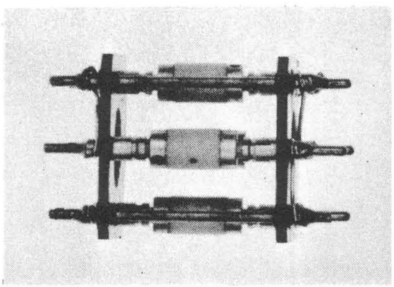

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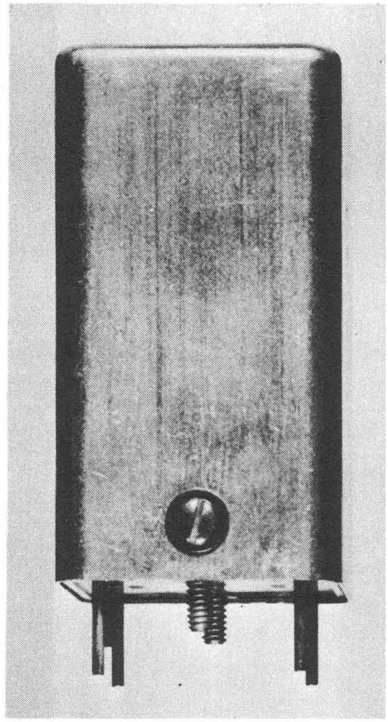

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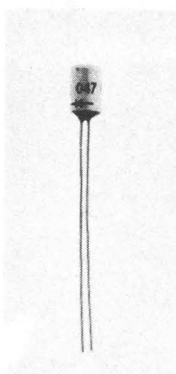

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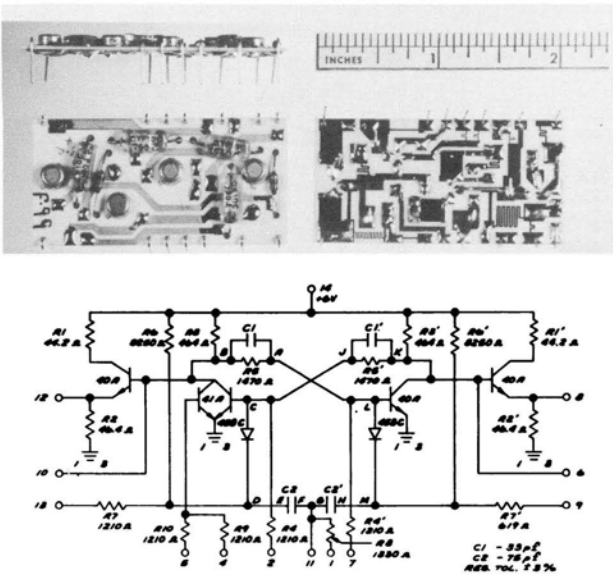
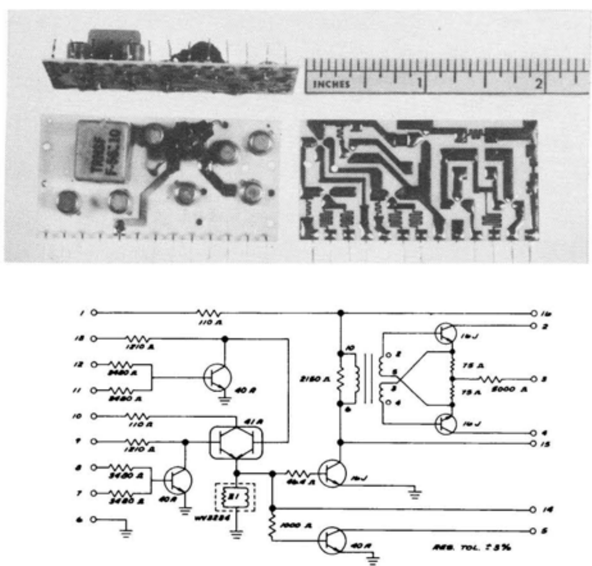
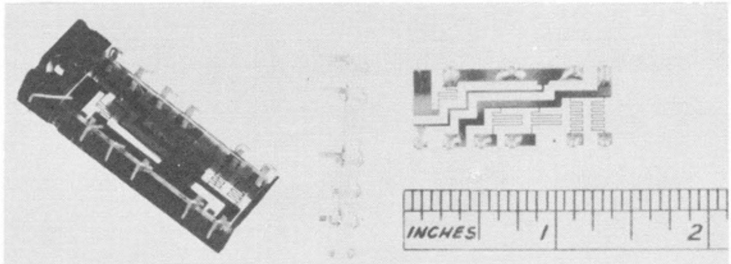
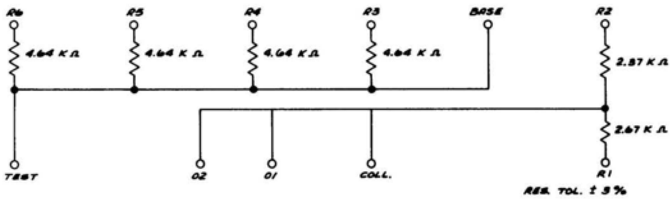


P-80 BINARY COUNTER AND SHIFT REGISTER

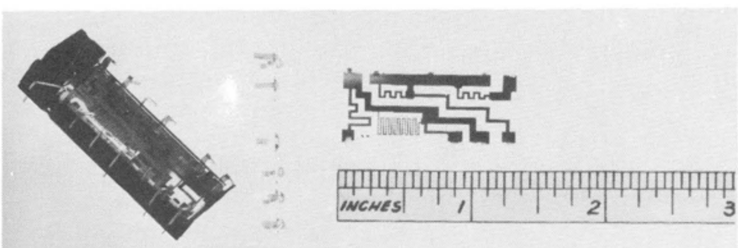


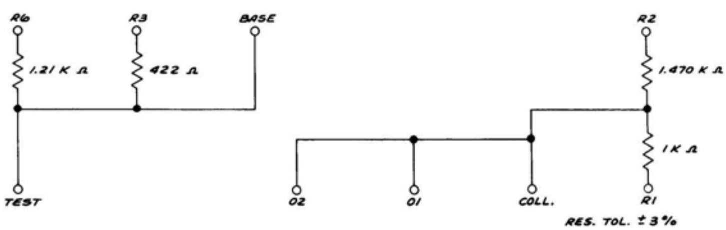
P-81 TIME DIVISION SWITCH



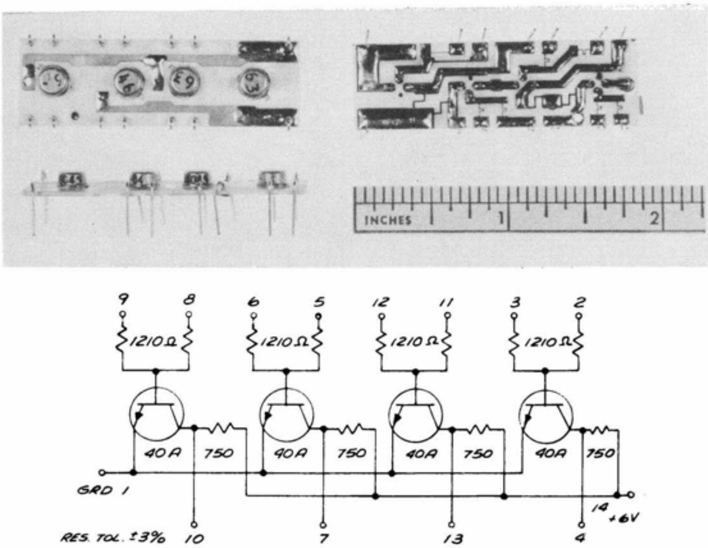


P-82 THIN FILM CIRCUIT PACK

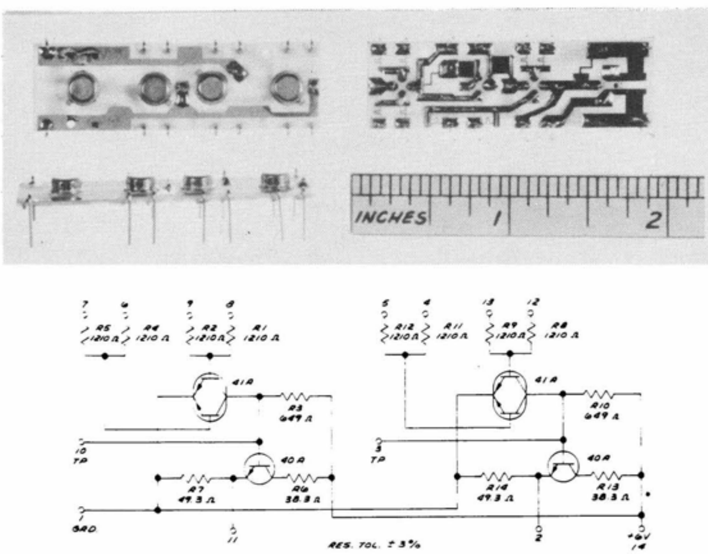




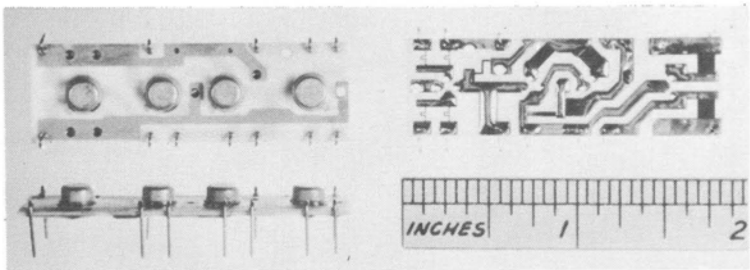
P-83 THIN FILM CIRCUIT PACK

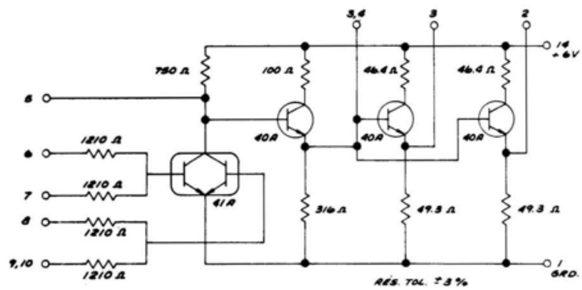


P-84 Four 2-INPUT GATE

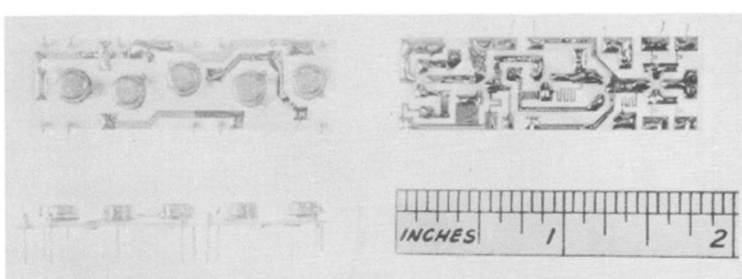


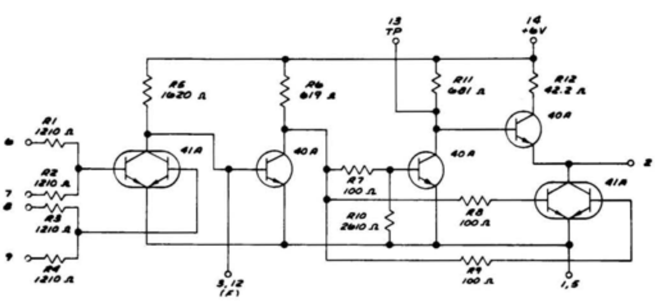
P-85 FOUR 4-INPUT GATE



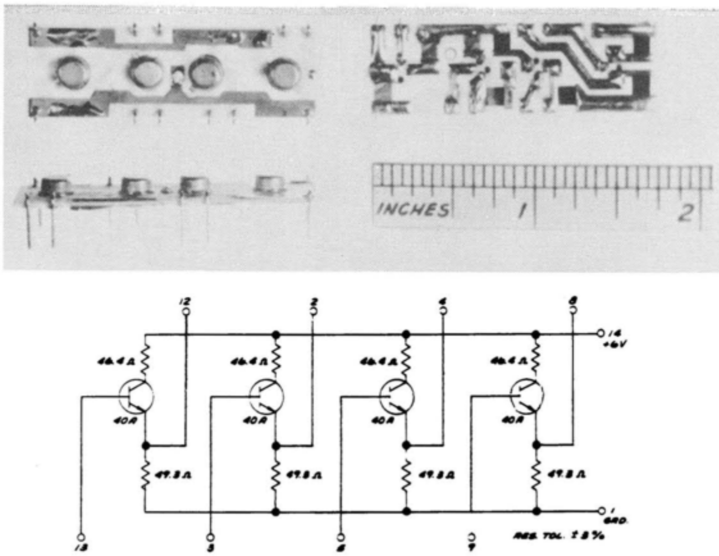


P-86 HIGH FAN-OUT

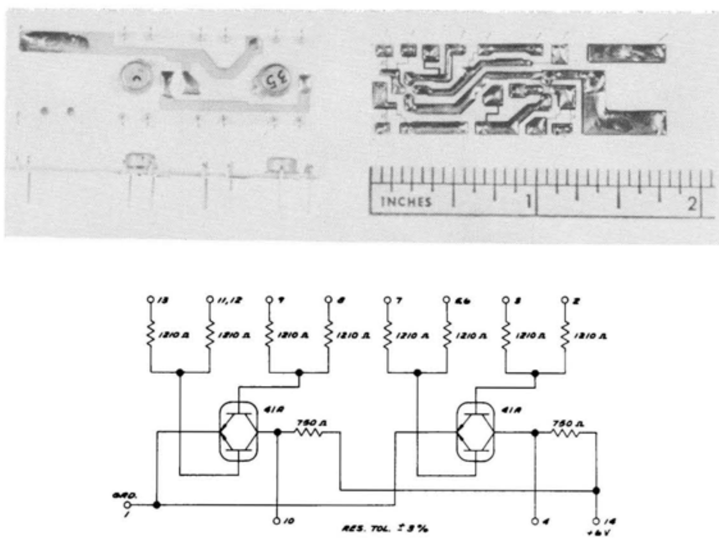




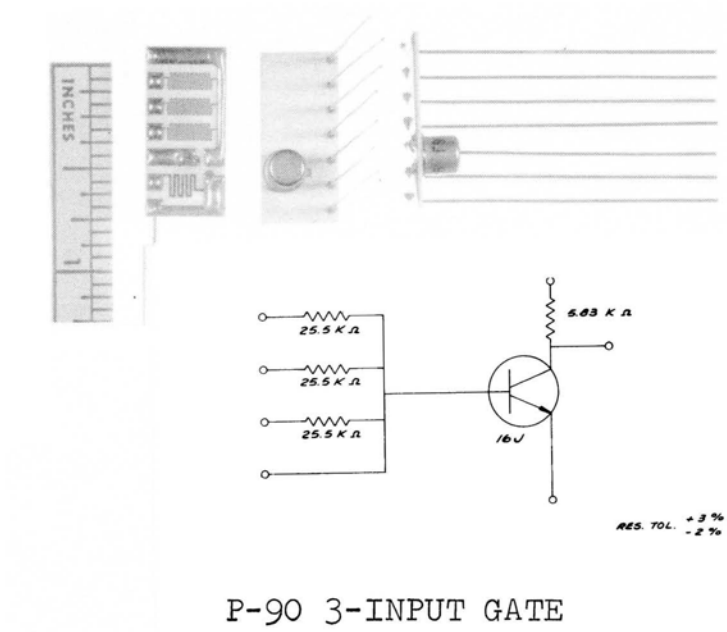
P-87 MODIFIED HIGH FAN-OUT



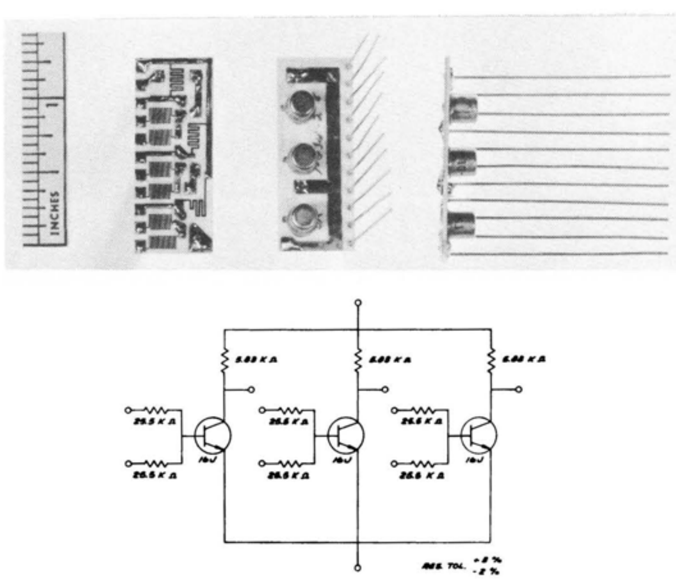
P-88 EMITTER FOLLOWER



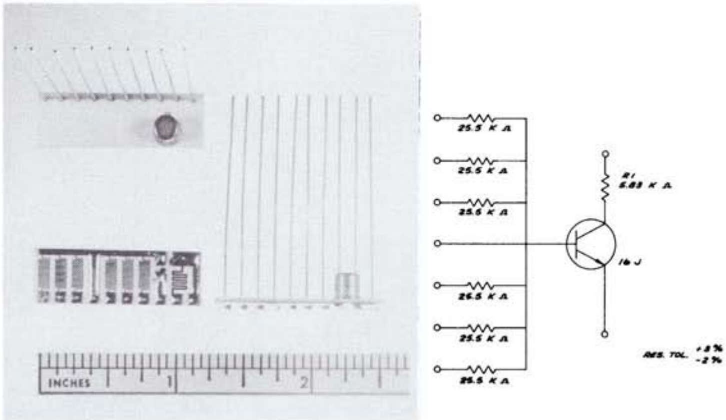
P-89 TWO 4-INPUT GATE



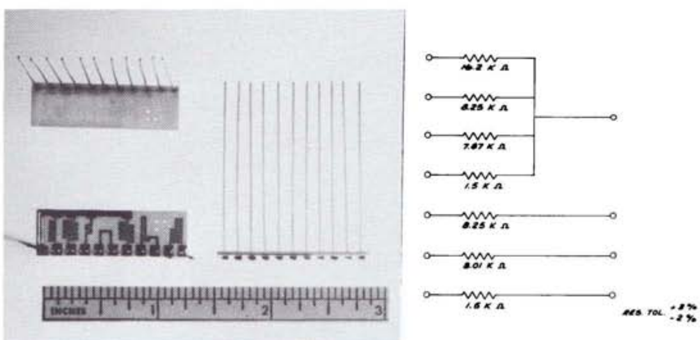
P-90 3-INPUT GATE



P-91 TRIPLE TWO-INPUT GATE



P-92 SIX-INPUT GATE



P-93 LINE CIRCUIT

Appendix A

GLOSSARY OF TERMS

BV.....Breakdown voltage

Breakdown voltage - That value of reverse voltage which remains essentially constant over a considerable range of current values.

BV_{CBO}.....Collector to base breakdown voltage, open emitter.

BV_{CES}.....Collector to emitter breakdown voltage, base dc short circuited to emitter.

BV_{EBO}.....Emitter to base breakdown voltage, open collector.

BV_F.....Forward breakdown voltage for PNPN devices.

The maximum forward voltage between E_P and E_N attained before breakdown under base bias conditions specified.

BV_R.....Reverse breakdown voltage for PNPN devices.

The maximum reverse voltage between E_P and E_N attained before breakdown is achieved or maximum specified reverse power is reached under base bias conditions specified.

C_O.....Capacitance of a diode at zero direct current.

The capacitance at a specified applied ac voltage and frequency and zero direct current.

fh_{fb}.....Small-signal short-circuit forward-current transfer ratio cutoff frequency.

The frequency at which the absolute value of the small-signal short-circuit forward-current transfer ratio is 0.70 times its value at the specified test frequency.

GLOSSARY OF TERMS (Continued)

f_T.....Extrapolated unity gain frequency.

The frequency, obtained by extrapolation, at which h_{fe} becomes unity when reduced at a rate of 6db/octave.

h_{fb}.....Small-signal short-circuit forward-current transfer ratio.

Definition - The ratio of the ac output current to the ac input current.

h_{FB}.....Static forward-current transfer ratio.

The ratio of the dc output current to the dc input current under the specified test conditions.

h_{fe}.....Small-signal short-circuit forward-current transfer ratio.

The ratio of the ac output current to the ac input current with zero ac output voltage.

I_{CBO}.....Collector cutoff (saturation) current, open emitter.

The collector cutoff (saturation) current is the dc leakage current in the collector or base terminal when it is reversed biased by a voltage less than the breakdown voltage and with the emitter dc open-circuited.

I_B.....Base current, dc.

I_F.....Forward current, dc.

I_H.....Hold current for PNPN devices.

The forward current at which the negative resistance across the device becomes equal to a specified value during the transition from the low impedance to the high impedance state under specified base bias conditions.

I_R.....Reverse current, dc.

GLOSSARY OF TERMS (Continued)

I_S.....Saturation current.

The dc reverse current which flows through the semiconductor diode under the reverse voltage conditions specified (normally 80% or less of BV).

N_F.....Noise figure.

At a selected input frequency the noise figure is the ratio of the total noise power per unit bandwidth (at the corresponding output frequency) delivered to the output termination, to the portion produced at the input frequency by the thermal noise of the input termination, whose noise temperature is standard (290°K) at all frequencies.

NRTM.....Not ready to manufacture. (Check use with Applications Engineer.)

Power Rating.....

That power, which, when applied under specific conditions, yields the junction temperature acceptable for a particular application. In the case of the Quick Selection Guide, the rating for silicon is 125 to 150°C and for germanium is 85 to 100°C with the case at 25°C or ambient as required.

Status.....

For convenience, the status is classified into two groups, as follows:

P.....Preferred.

R.....Restricted (check use with Applications Engineer).

$t_d + t_r$.....Pulse delay plus rise time.

The time interval from a point at which the leading edge of the input pulse has risen to a specified part (normally 10%) of its

GLOSSARY OF TERMS (Continued)

maximum amplitude to a point at which the leading edge of the output plus has risen to a specified part (normally 90%) of its maximum amplitude.

t_s.....Pulse storage time.

The time interval from a point at which the trailing edge of the input pulse has decreased a specified part (normally 90%) of its maximum amplitude to a point at which the trailing edge of the output pulse has decreased to the same specified part of its maximum amplitude.

$t_s + t_f$.....Pulse storage plus fall time.

The time interval from a point at which the trailing edge of the input pulse has decreased a specified part (normally 90%) to a point at which the trailing edge of the output pulse has decreased to a specified part (normally 10%) of its maximum amplitude.

t_{rr}.....Reverse recovery time.

The time between the instant of current reversal from forward to reverse and the instant at which the specified reverse condition is reached.

V_{BE}.....Base to emitter voltage.

$V_{CE}(sat)$.....Saturation voltage, collector to emitter.

The dc voltage between the collector and emitter terminals for the specified saturation conditions, (when the transistor output characteristic is essentially a constant voltage).

$V_{CE}(sus)$.....Sustain voltage, collector to emitter.

The voltage which appears between the collector and emitter terminals with specified input current or voltage and output current. (LV_{CEO})

GLOSSARY OF TERMS (Continued)

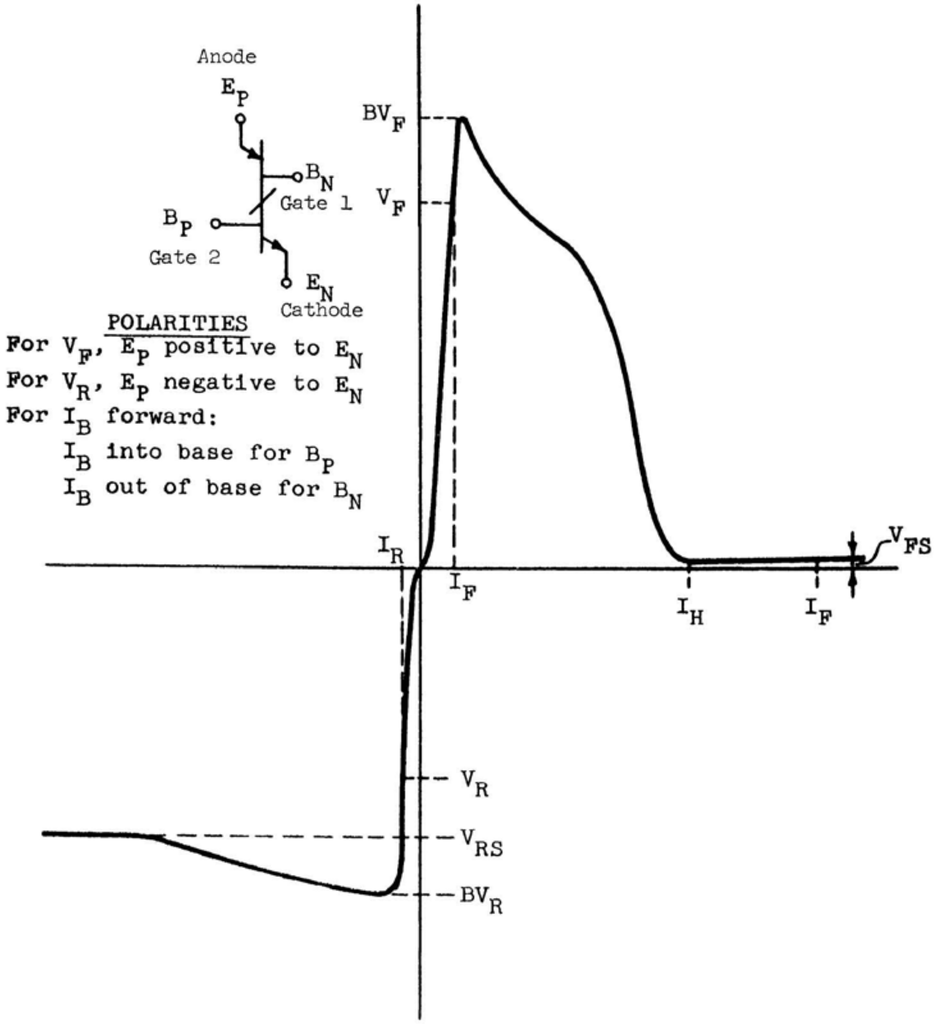
V_F.....Forward voltage, dc.

V_R.....Reverse voltage, dc.

V_{RT}.....Reach through voltage.

That value of reverse voltage for which the depletion layer spreads sufficiently to contact another junction or contact.

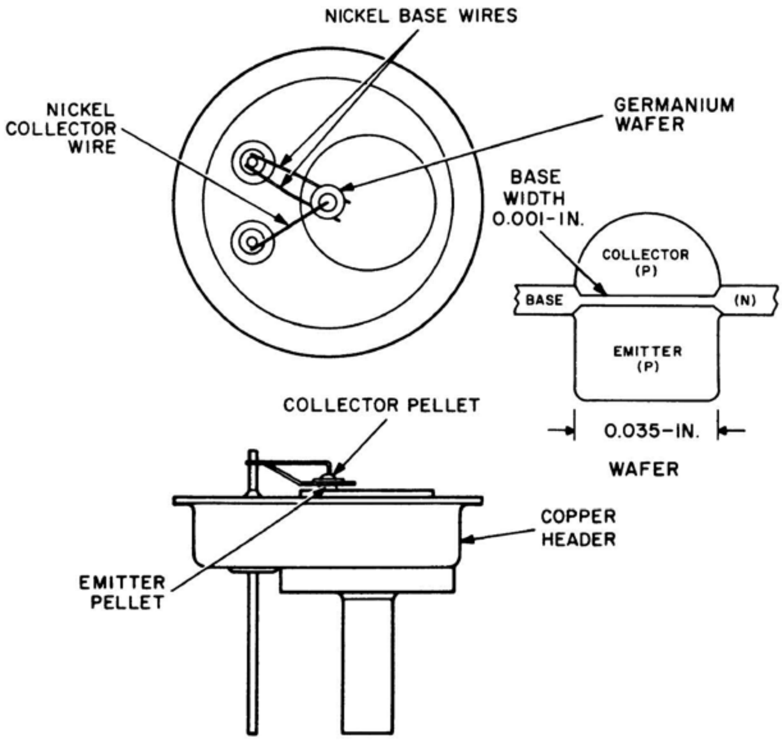
Following is a graphical presentation of symbols for multiple junction devices:



Appendix B

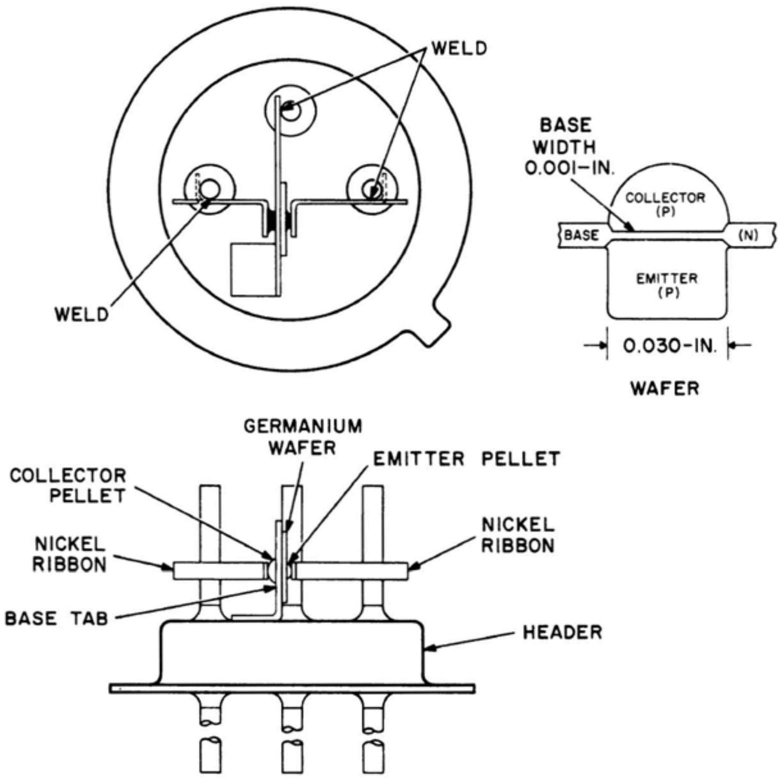
TYPICAL TRANSISTOR AND DIODE CONSTRUCTION

The illustrations on the following pages show the internal construction of some basic transistors and diodes manufactured by the Western Electric Company. Note the minute dimensions of the active regions. Consult the data sheets for electrical ratings. (All dimensions shown on illustrations are approximate.)



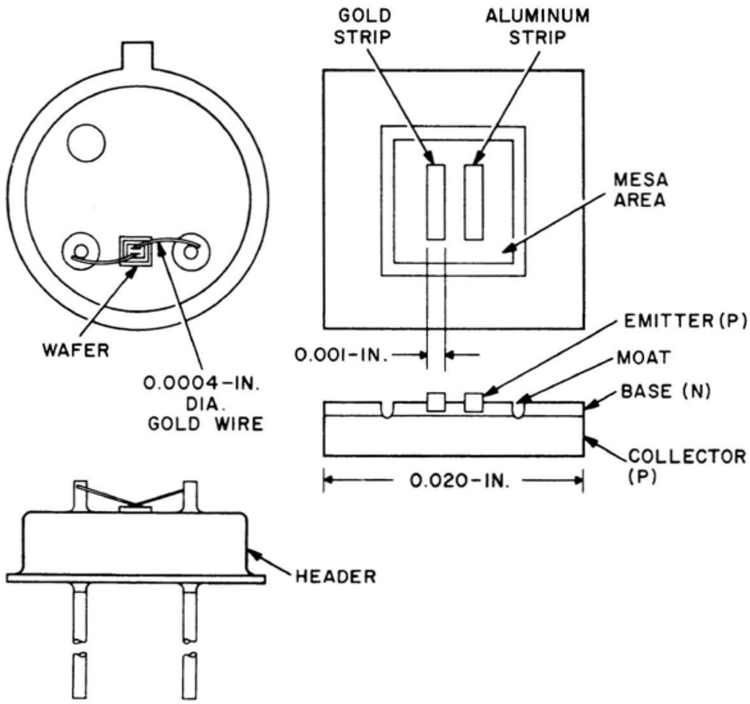
PNP MEDIUM POWER GERMANIUM ALLOY TRANSISTOR - 9 B, D TYPE

The 9 B, D transistor is suitable for use in medium-power, low-distortion amplifier, medium-speed switching and core-driving applications.



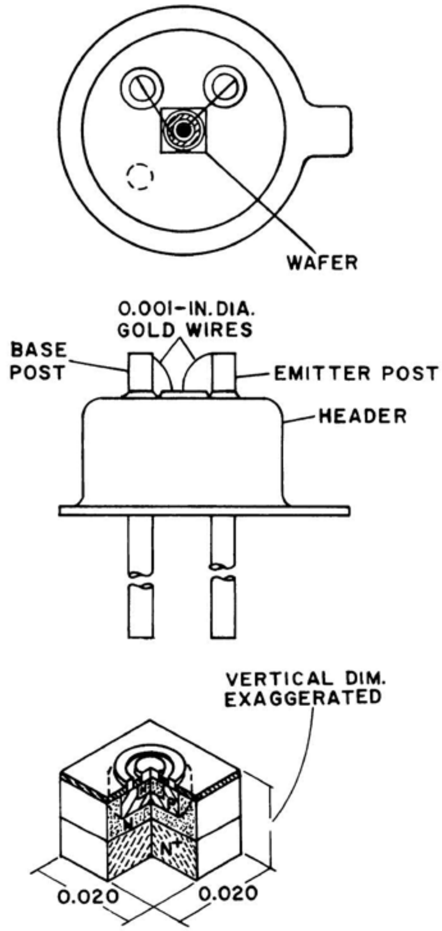
MILLIWATT GERMANIUM ALLOY PNP TRANSISTOR - 12 TYPE

The 12-type transistor is a 1/4-watt, general purpose, PNP germanium alloy junction transistor. It is used principally as a medium-frequency amplifier or medium-speed switch.



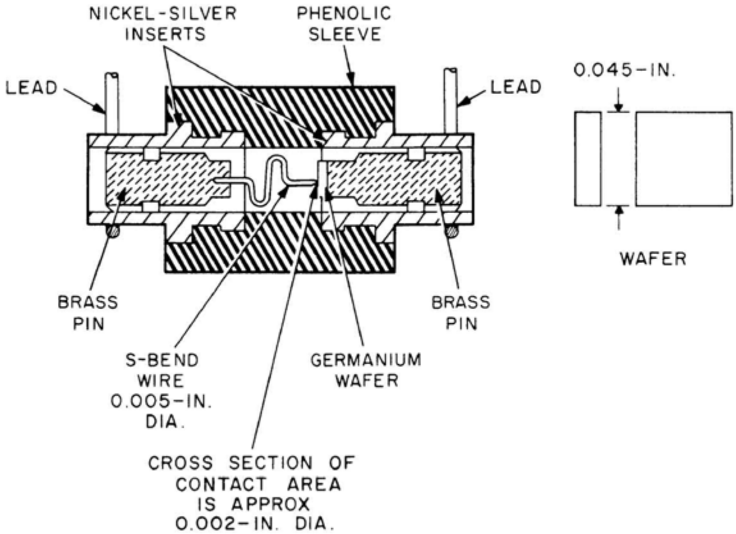
MILLIWATT GERMANIUM DIFFUSED BASE (ULTRA-HIGH FREQUENCY) PNP TRANSISTOR - 15 TYPE

The 15-type transistor is used principally as a VHF amplifier or very fast switch.



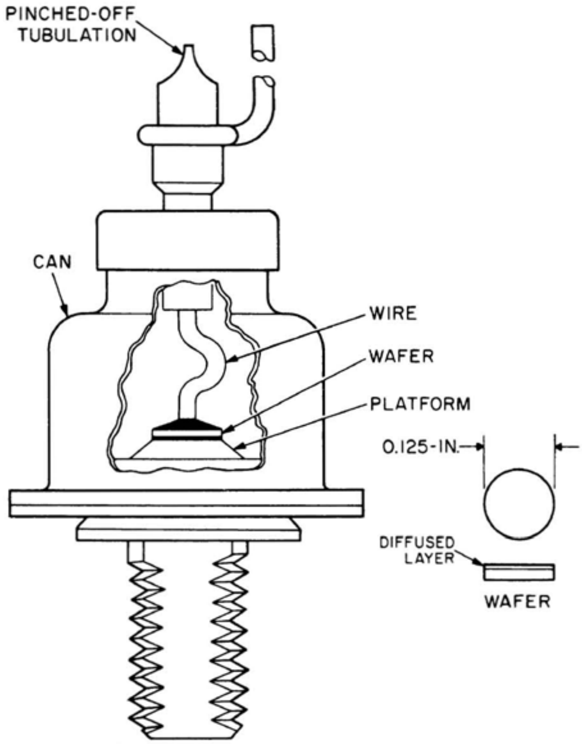
NPN MILLIWATT SILICON DIFFUSED
TRANSISTOR - 16 TYPE
(PLANAR)

The 16-type transistor is used principally as a general purpose, radio-frequency, small-signal amplifier or high-speed switch.



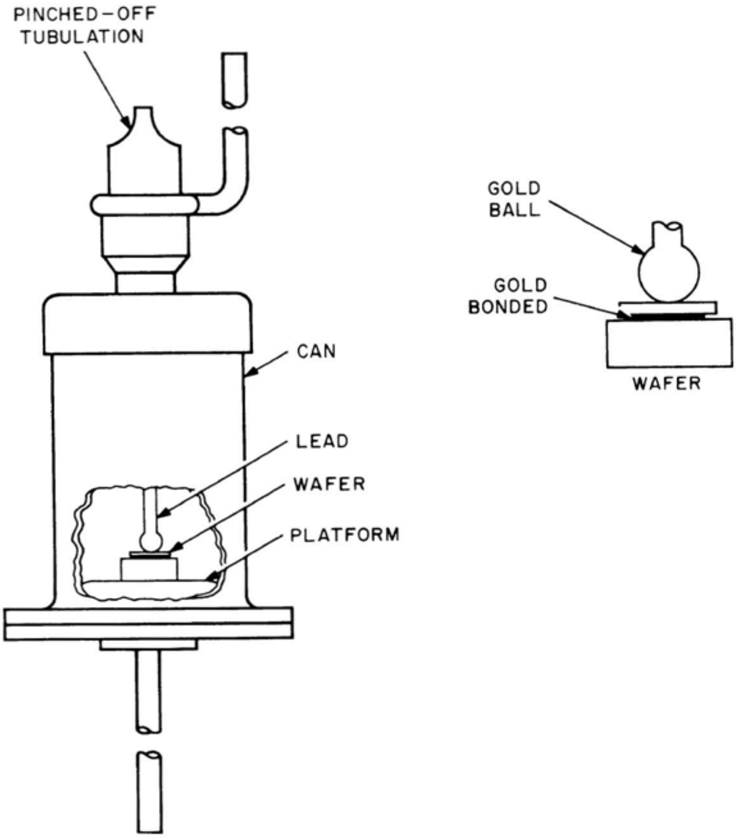
POINT-CONTACT DIODE - 400 TYPE

The 400-type is a general purpose diode used principally as a detector or low-power rectifier. The 441-type diodes are electrically identical to the 400-type, except that they have axial leads.



HIGH POWER SILICON DIFFUSED JUNCTION
DIODE - 425 TYPE

The 425-type diode is used principally as a high-power rectifier or voltage regulator, capable of dissipating 10 watts when properly heat-sinked.

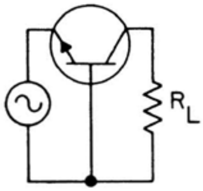
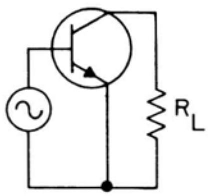
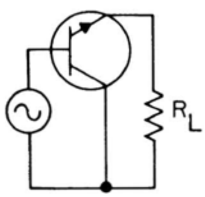


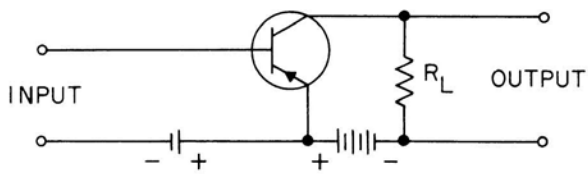
MEDIUM POWER SILICON DIFFUSED JUNCTION
DIODE - 426 TYPE

The 426-type diode is used principally as a medium-power rectifier, or voltage regulator.

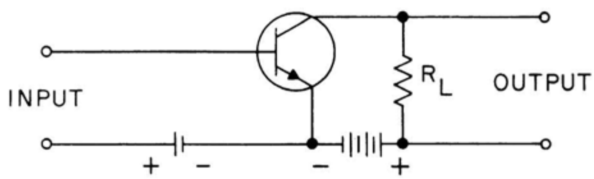
Appendix C

Transistor Circuit Configurations

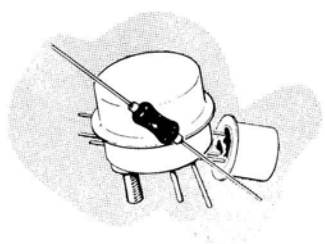
CIRCUIT	CHARACTERISTICS
 COMMON BASE (CB)	Lowest input impedance Highest output impedance Low current gain (<1) High voltage gain Moderate power gain
 COMMON EMITTER (CE)	Moderate input impedance Moderate output impedance High current gain High voltage gain Highest power gain
 COMMON COLLECTOR (CC) (EMITTER FOLLOWER)	Highest input impedance Lowest output impedance High current gain Unity voltage gain Lowest power gain



COMMON EMITTER BIAS CIRCUIT - PNP



COMMON EMITTER BIAS CIRCUIT - NPN



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