Section 4

SECTION IV

COMPONENT DESCRIPTION

CONTENTS PAGE

Figures

Tables

1. GENERAL

1.01 This section contains detailed block diagram level discussions on the individual plug-in units that make up the B325 channel bank.

2. ALARM AND POWER UNIT (325AP01)

2.01 The alarm and power unit block diagram is shown in Fig. 1. A control panel, which is part of the unit, provides mounting for system fuses, indicators and maintenance switches. Control panel controls and indicators are detailed in Fig. 2, Section I of this manual. Alarm and power unit circuitry is designed to perform four basic functions:

(a) Convert -50 (±6) volts dc office supply voltage to regulated +5-volt and unregulated +12 and -12-volt dc levels for channel bank operation.

(b) Output service-interrupting alarm indications to the central office and indicate alarm-creating malfunction on panel-mounted indicators.

(c) Output carrier group alarm (CGA) trunk-conditioning signals to stop customer charges and make trunks busy during the alarm period.

(d) Provide circuit-configuration change for maintenance and alignment of the channel bank.

2.02 The internal logic power supply is rated at 1 ampere for the +12-volt and -12-volt outputs and 0.6 ampere for the 5-volt output. Maximum ripple voltage is 100 millivolt on any output. Voltage regulation is ±5 percent for the 5-volt output. Short-circuit protection is provided by inhibiting the dc-to-dc converter in the presence of an overload. Automatic start-up is attempted every 4 to 5 seconds, ensuring power restoration once the overload is removed.

2.03 Dry-contact relay closures are provided for activation of central office visual and audible alarms. Two contact sets of relay K1 are output to the circuit board connector for connection to the central office at terminal installation. The office alarm circuits also contain contacts of relay K2. These contacts provide bypass and interruption functions, which deactivate office alarms when the ACO switch is pressed. Relay K1 is normally held energized by the trunk processing circuitry and is dropped out when an alarm condition occurs. When relay K1 drops out, a circuit is created to energize relay K2 via the ACO switch. Once energized, relay K2 is latched until the alarm is cleared and relay K1 energizes again.

2.04 Remote alarms are detected by an integrator circuit, which monitors a Bit-2 sampling (DACIN 2F) of each channel's decoded 8-bit parallel data word from the receive converter. If Bit 2 has been forced to zero in each data word at the far end, DACIN 2F will be a standing high-logic level. The integrator circuit will drive the REM line high (true), if DACIN 2F remains high for 450 (±80) msec. This triggers the trunk processing circuits to provide CGA conditioning outputs and de-energize relay K1. A REM alarm indicator will come on whenever the REM line is high, if a local alarm is not presently active.

2.05 Local alarms are detected by a similar integrator circuit, which monitors out-of-frame (OOFH); and receive clock loss (RCKLSH) signals from the receive converter and an internally generated fuse or power-fail signal. The local alarm integrator may be strapped for a 280 (±40) msec or a 2 (+0 -0.5) second alarm detection period. Detection of a local alarm also triggers the trunk processing circuits and turns on the LOC alarm indicator, as well as a FRAME, or RCLK, and/or FUSE PWR FAIL indicator. The alarm detection and indicator circuits have priority control built in; whereas, detection of a local alarm will override and inhibit detection of a remote alarm, and a receive clock-loss signal will inhibit illumination of the FRAME indicator.

2.06 The trunk processing unit outputs time-controlled signals to make all trunks busy and stop subscriber charges during an alarm period. The unit provides an initial (first) timing sequence and a termination (second) timing sequence for local alarms, and only a first timing sequence for remote alarms. As remote alarms are generated from a local alarm at the far end, termination timing is controlled from there, maintaining the slave (remote) to master (local) relationship. The first timing sequence period in strap selectable for a

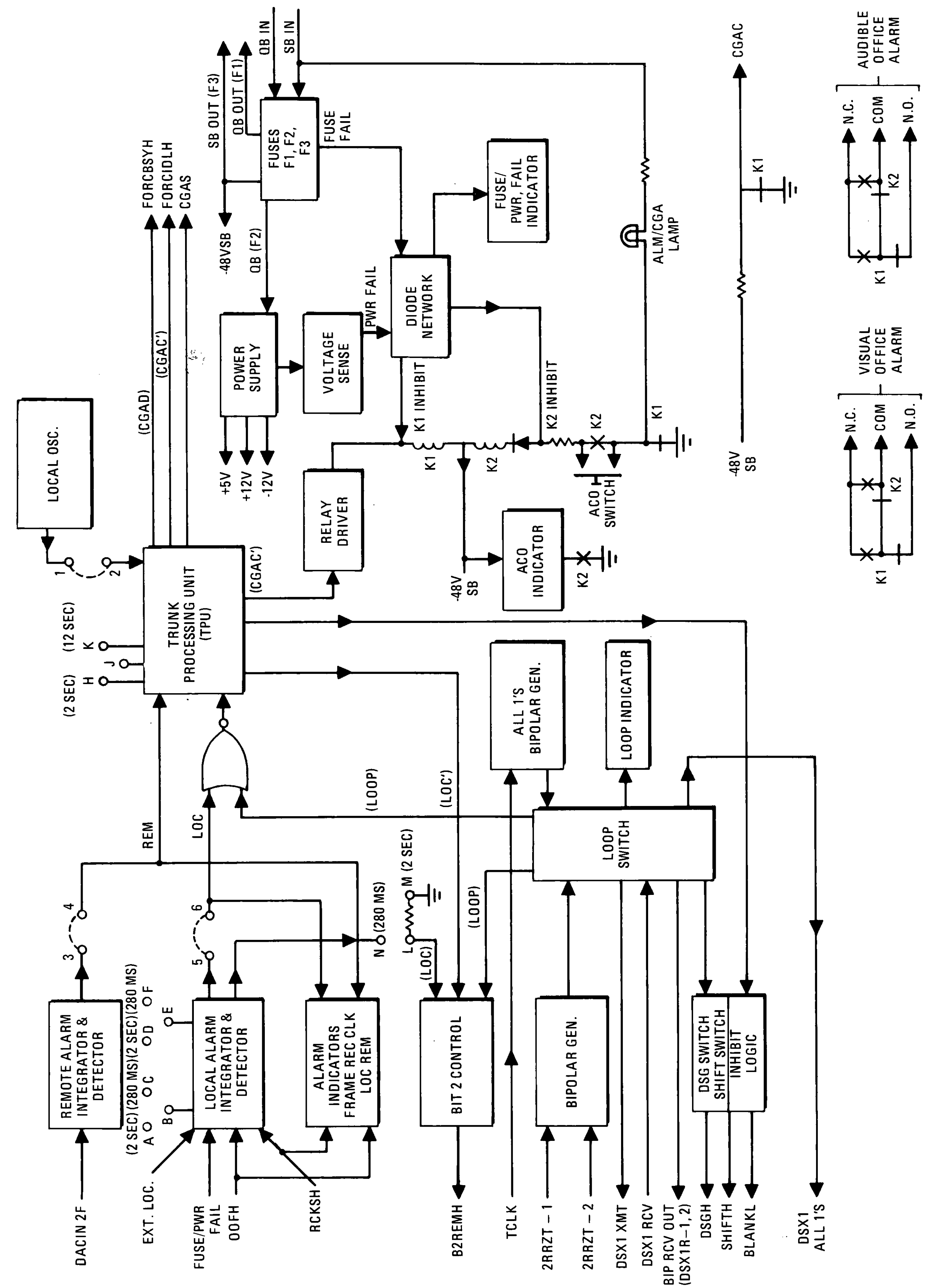

Fig. 1—Alarm and Power Unit Block Diagram

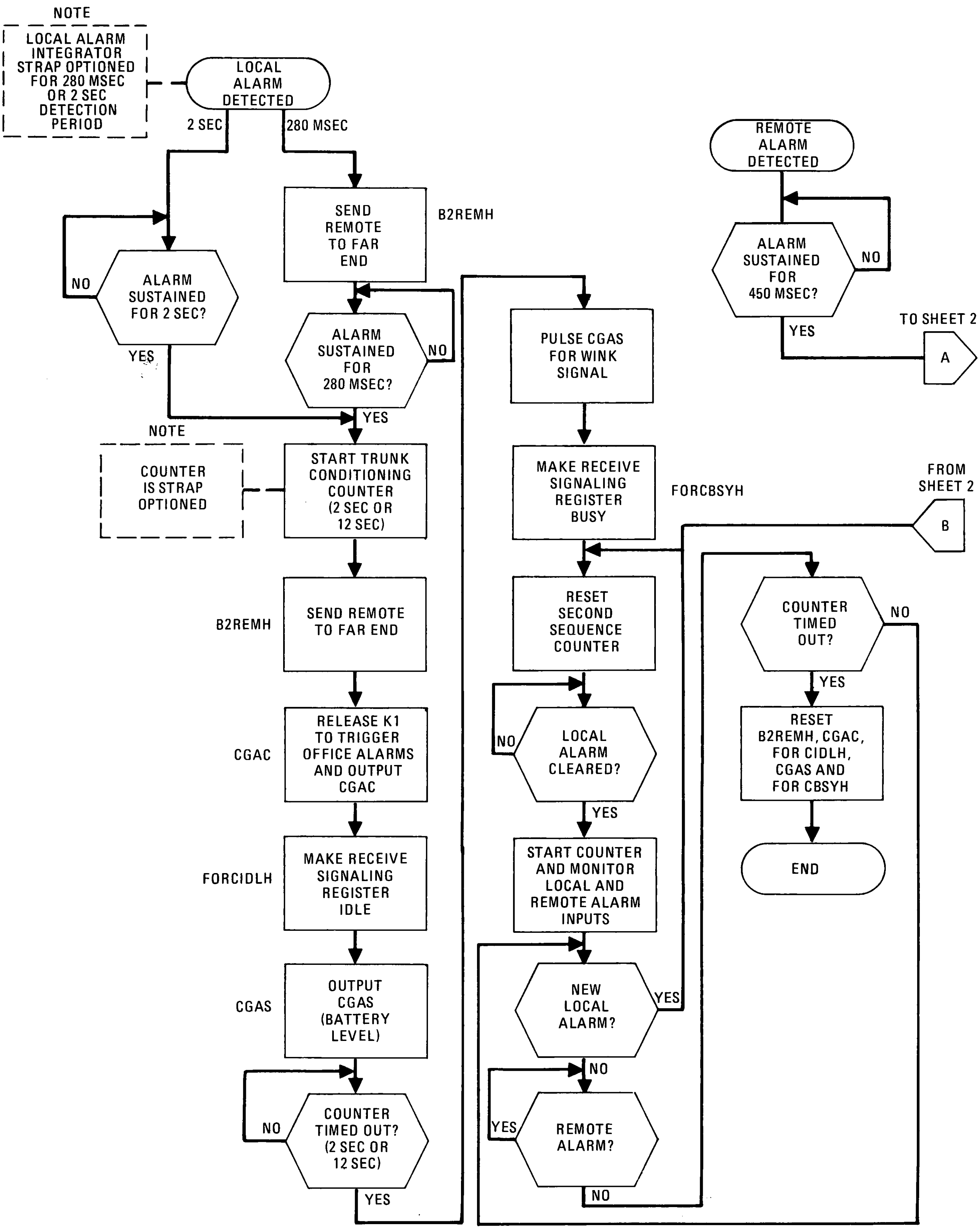

Fig. 2—CGA Trunk Processing Flow Chart (Sheet 1)

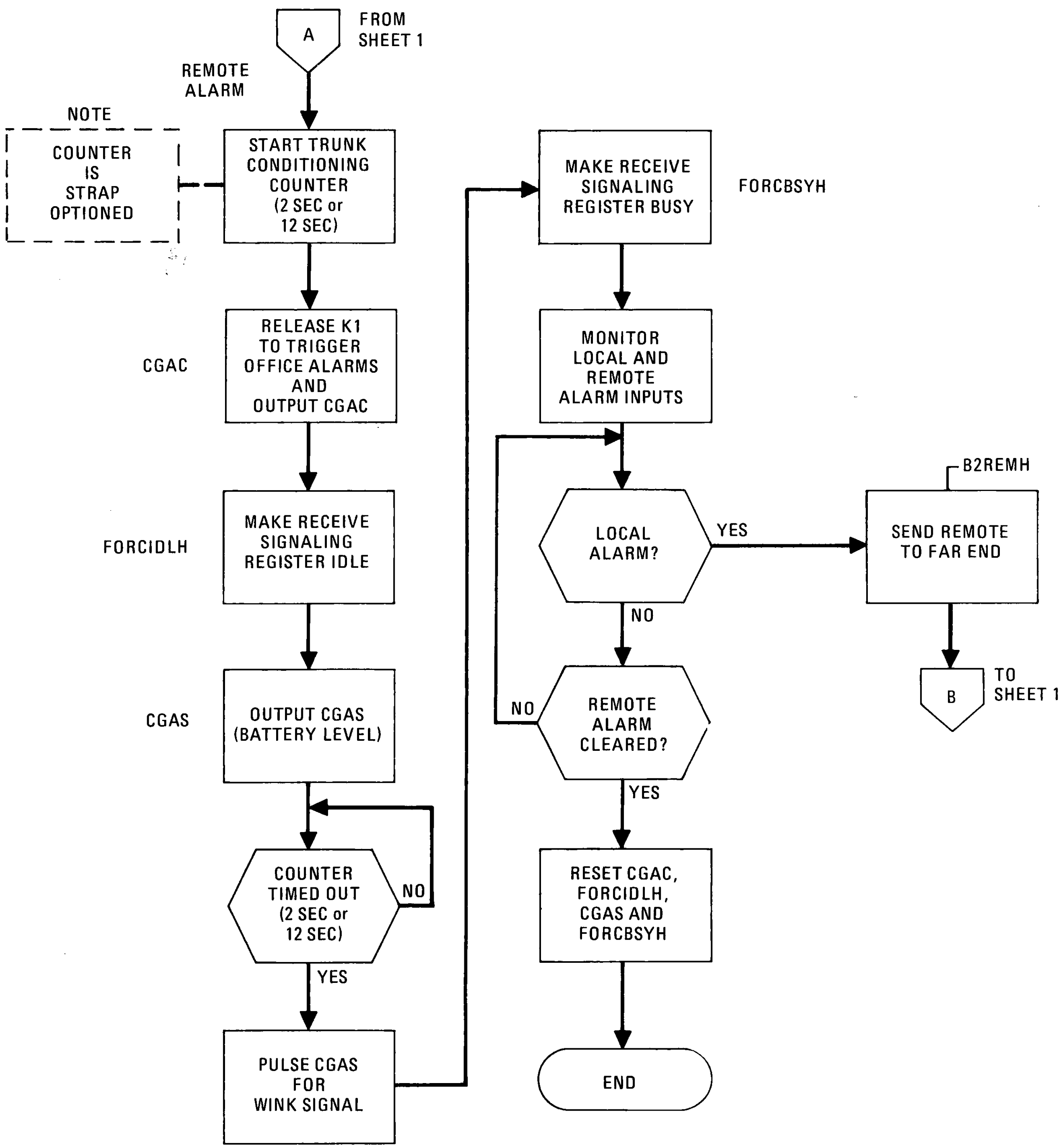

Fig. 2—CGA Trunk Processing Flow Chart (Sheet 2)

2-second or 12-second trunk processing sequence. The second timing period is a 12-second delay. This is compatible with present and future Bell requirements.

2.07 The first timing sequence is basically the same for a local alarm or remote alarm. The only difference being that a remove Bit-2 (B2-REMH) command is sent to the transmit converter during local alarms only. This signals the transmit converter to send a remote alarm to the far end. The following steps summarize alarm sequence operations.

(a) Alarm detection (through first sequence)

(1) Inhibit receive VF reception and make receive signaling idle on all channels.

(2) Output CGAC to busy required channel units and trigger office alarms.

(3) For local alarms only, transmit remote alarm to far end.

(4) After first sequence time-out, produce wink signal to drop subscribers, then busy receive signaling on all channels.

(b) During alarm period, maintain conditions established in Step (a).

(c) When alarm clears

(1) For local alarms only, after second sequence time-out, reestablish normal conditions.

(2) For remote alarms only, reestablish normal conditions immediately.

2.08 The first alarm timing sequence is guaranteed to completion, regardless of alarm duration. The second sequence may be reset to time zero by a local alarm that disappears then reappears during the second sequence. As an example, for 12-second trunk-processing strapping, a local alarm that lasted for 3 continuous seconds would produce a total alarm sequence period of 24 seconds; whereas, a local alarm that lasted for 3 seconds, disappeared for 17 seconds, then reappeared for 2 seconds would produce a total alarm sequence period of 34 seconds. A flow chart describing trunk-processing unit logic functions is contained in Fig. 2.

2.09 Maintenance switch complement consists of a loop switch, a digital signal generator (DSG) switch and a shift switch. Actuation of the LOOP switch loops the transmit signal back into the receive path, applies termination load to the incoming signal from the far end, and connects a bipolar all-ones signal generator to the transmission line. In addition, VF blanking functions are inhibited so the receive channels will be operational for VF adjustment and maintenance.

2.10 Actuation of the DSG switch sends a digital signal generator (DSGH) command to the receive converter. This forces the receive converter to output a standard 1-kHz 0-dBm digital test signal in the receive path.

2.11 Actuation of the SHIFT switch sends a SHIFT command to the receive converter to shift the receive channel VF forward by eight channel positions

3. TRANSMIT CONVERTER (325TC01)

3.01 The transmit converter is shown in Fig. 3. Logic supply-voltage test jacks are leading edge-mounted for easy access during maintenance testing. The unit is constructed with two circuit boards, one mounted piggyback to the other. Unit logic circuitry is primarily composed of state-of-the-art integrated circuit devices, including some CMOS devices. Although highly reliable when installed in operational circuits, CMOS devices have some susceptibility to static discharge damage in the unconnected circuit condition. For this reason, the unit requires some care in handling; and when removed, it should always be stored in the Velostat (antistatic) bag in which it was shipped.

3.02 All operations of the transmit converter are synchronized by signals generated from a 6.176-MHz clock which may be strapped to operate phase-locked to the receive-converter input signal or as an internally generated source. The transmit converter accepts 24 parallel channels of VF and signaling from the channel units and outputs serial, two-rail, return-to-zero (RTZ) data at a 1.544-megabit/second rate. Conversion to the 1.544-Mbps

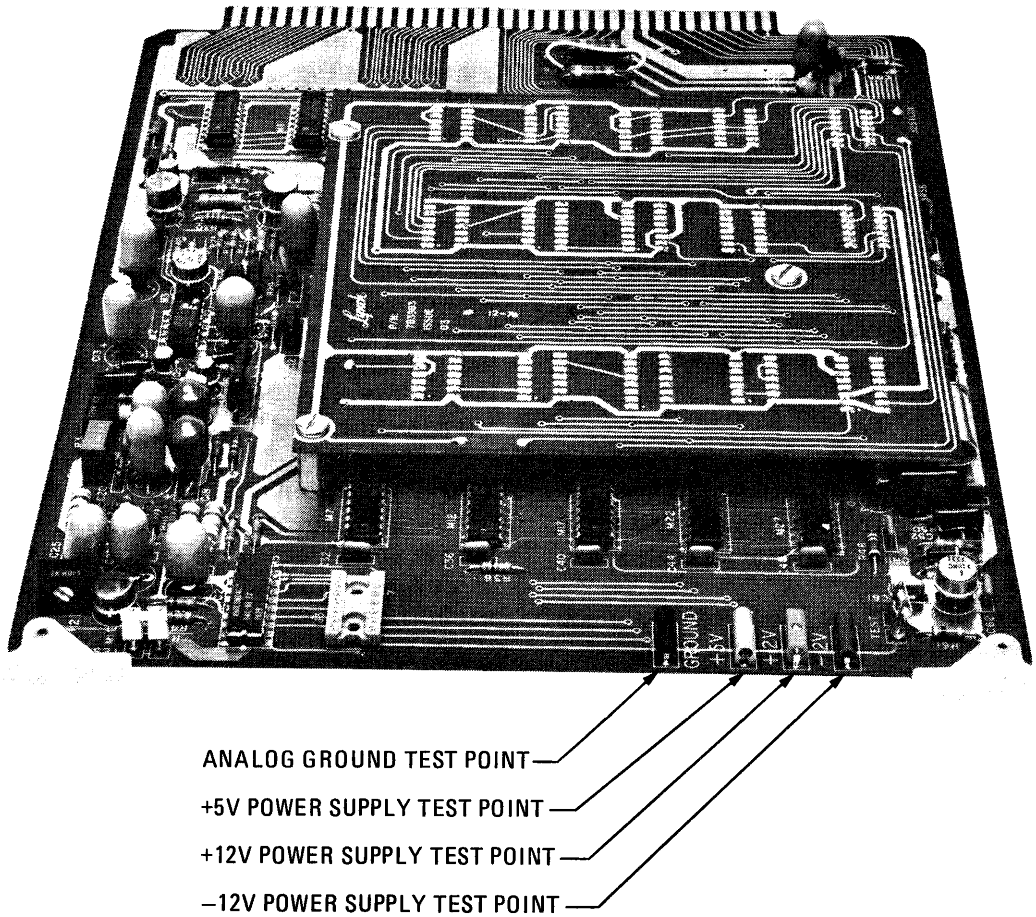

Fig. 3—Transmit Converter (325TC01)

bipolar (DSX-1 format) output signal is accomplished in the alarm and power unit (325AP01).

3.03 The 24 VF channels are sampled 8000 times a second by three eight-line multiplexers. Signaling is sampled in the same manner. Output of the VF multiplexers is fed to an analog-to-digital coder circuit.

3.04 The basic translation of the analog samples to an eight-bit digital word is accomplished by a successive approximation coding. The first bit in this word is used to signify the analog signal polarity; the remaining seven bits are used to convert 128 discrete voltage levels to their binary equivalent.

3.05 The coding scheme is somewhat modified by a companding digital-to-analog converter (COMDAC), which is used to realize the u = 255 PCM companding law. The COMDAC provides compression of the analog signal, taking into account that the normal distribution of voice energy is at the lower analog levels. Hence, under the influence of the COMDAC, the coder's output digital word is nonlinear, to provide more definition at the lower analog levels and to reduce quantizing distortion.

3.06 The 8-bit parallel A/D converter output is applied through zero suppression circuits to a parallel-to-serial converter. The zero suppression circuits examine each parallel data bit to ensure at least one logic "1" appears in a data word. If the word contains all logic zeros (0), a logic "1" is automatically inserted in the LSB position. This is done to enhance clock recovery in span line repeaters.

3.07 Zero suppression circuits also provide entry points for remote alarm and signaling data inputs. A remote Bit-2 discrete from the alarm and power unit will clamp the second most significant bit (MSB) of the data word to logic "0," creating a remote alarm transmission to the far end. A signaling data bit is gated into every channel word LSB position every sixth data frame, as determined by frame-bit generation circuits. These circuits produce a reoccuring frame-bit sequence code (as shown in Fig. 4) composed of main-frame synchronization reference bits and sixth frame (signal frame) identification bits. The receive converter at the far end will check for alternating main-frame bits spaced 386 bits apart to validate synchronization. Signaling frame bits are an alternating 111-000 pattern, allowing separation of A and B signaling, used by foreign exchange (FX) channel units. A-signaling follows the 111 frame-bit sequence, and B-signaling follows the 000 frame-bit sequence. The transmit converter transmits signal-clock output transitions on the 111/000 sequence, producing a 666.7-Hz square wave signal that is used to encode the FX channel unit signaling.

4. RECEIVE CONVERTER (325RC01)

4.01 The receive converter is shown in Fig. 5. Like the transmit converter, operational circuitry is composed primarily of integrated circuit devices, including some CMOS devices that require special care in storage and handling.

4.02 See Fig. 6. Receive converter circuits reverse the process that occurred in the transmit converter to recover the original PAM signal. The incoming bipolar signal is converted to a unipolar NRZ signal. A ringing tank, similar to that used in a T-1 repeater, provides clock recovery. The 1.544-MHz clock derived by this circuit is used to time all conversion functions within the unit and is also output to the transmit converter as a clock sync signal, where it can be used to phase lock the transmit clock as noted in Paragraph 3.02. Several conditions, including clock loss and loss of frame, are monitored on the receive converter and given to the alarm and power unit local alarm circuitry for alarm processing.

4.03 The unipolar VF data signal is retimed by the recovered clock, converted to parallel format, and applied to a companding digital-to-analog converter. This produces a time-division multiplex PAM signal, which is routed to three eight-line demultiplexers on the same card. The demultiplexers are gated to sample the PAM bus in proper sequence (1-through-24 order for D3 format), at appropriate times. Resulting samples are routed to corresponding channel units, where integration circuitry recovers the voice signal.

4.04 Signaling data is extracted from the LSB output of the serial-to-parallel converter and gated into a 24-bit shift register through control gates, which are enabled by a signal frame-sequence detector. Signaling outputs are also affected by alarm condition inputs from trunk-conditioning circuitry in the alarm and power unit. Force-busy and force-idle signals reset the shift register and inhibit signaling gating, respectively, to create the busy and idle conditions.

4.05 Bit-2 (second MSB) of the data messages is also extracted at the output of the serial-to-parallel converter and is continually applied to the alarm and power unit for detection of a remote alarm from the far end.

4.06 Out-of-frame detection circuits provide discrete outputs to inhibit VF and signaling paths, while framer circuits resynchronize the input bit-stream. This is done by checking main-frame reference bits for an alternating one-zero (1-0) sequence and enabling the VF and signaling outputs, when the bit stream is back in frame. Typically, reframing occurs in 11 milliseconds or less. A receive signal clock output is applied to FX channel units for decoding of A and B signaling.

4.07 A "digital milliwatt" or 1-kHz 0-dBmO digital generator is a standard test feature in the receive converter and is controlled from the alarm and power unit, when the channel bank is in a loop mode. Outputs from the digital generator replace PCM signals as inputs to the serial-to-parallel converter. This provides a standard signal for test and alignment of the channel units.

5. CHANNEL UNITS

5.01 The eight different channel units available for use in the B325 terminal may be categorized and discussed in terms of operational groups. These groups are: standard transmit and

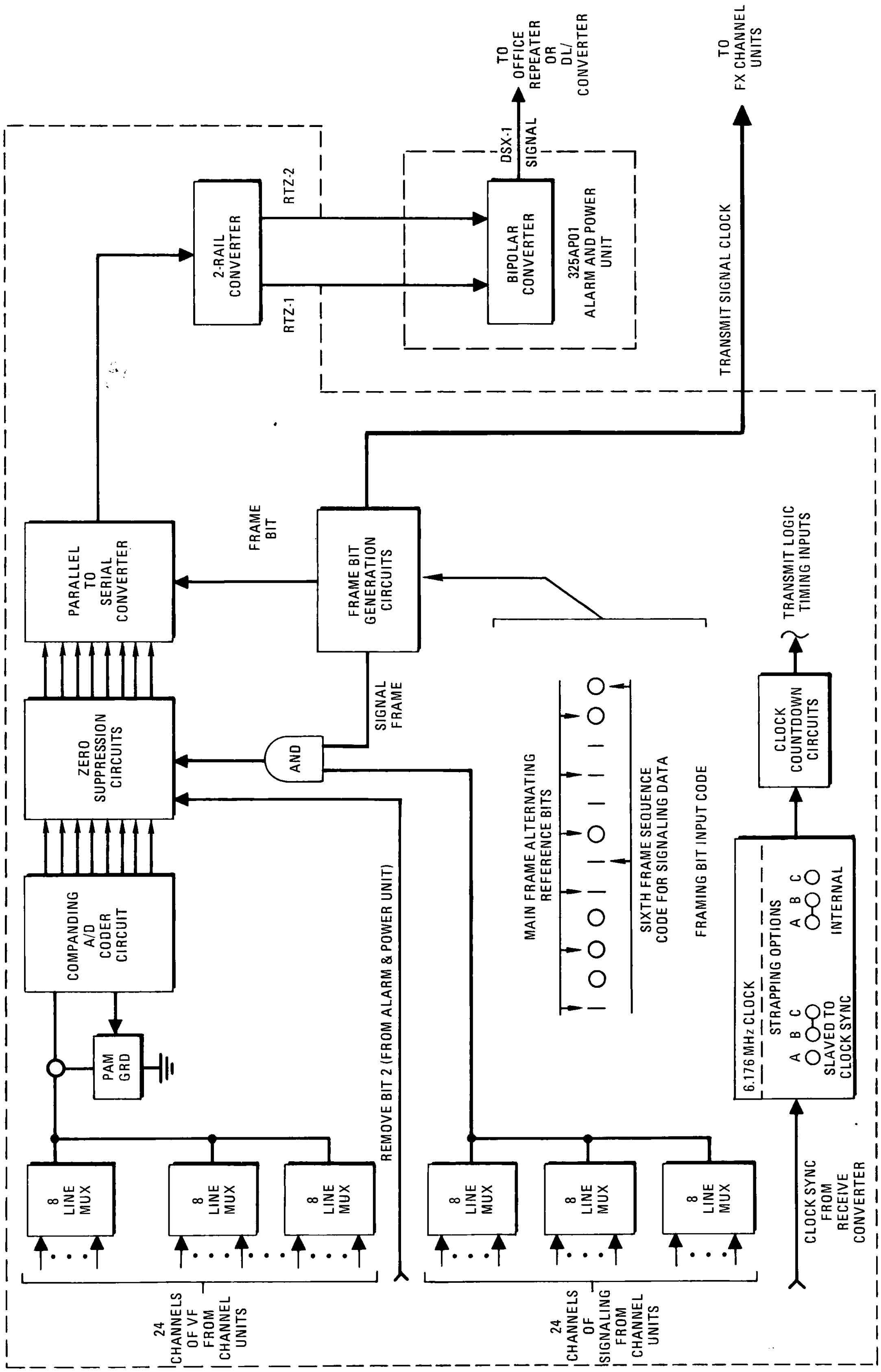

Fig. 4—Transmit Converter Block Diagram

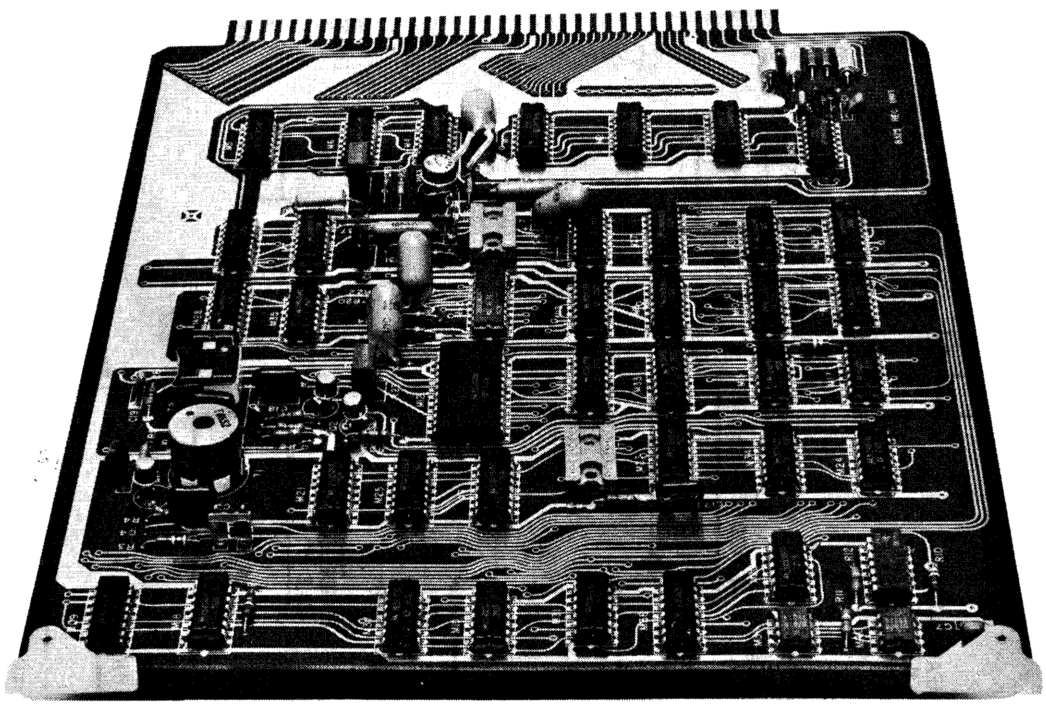

Fig. 5—Receive Converter (325RC01)

receive (E&M) channel units, dial pulse (DP) channel units, voice frequency (VF) only channel units, and foreign exchange (FX) channel units. All channel units are equipped with color-coded edge-mounted test jacks for ease of maintenance/ alignment and have strapping options clearly decaled on the circuit board component side. A typical channel unit is shown in Fig. 7.

E&M CHANNEL UNITS (325EM01, 325EM02, 325EM03)

5.02 The E&M channel units are all two-way speech and signaling units that work end-to-end with any other E&M channel unit. Variations of the basic channel unit provide for 4-wire/ 600-ohm connection (325EM01), 2-wire/600-ohm connection (325EM02), and 2-wire/900-ohm connection (325EM03). Voice-frequency signals are filtered by a 180-Hz to 3450-Hz bandpass filter in the transmit direction and a 3450-Hz low pass filter in the receive direction. In addition, the two-wire units may be obtained with optional A-lead and B-lead signaling circuits installed. See Fig. 8 for a block diagram of 2-wire E&M channel units and Fig. 9 for a block diagram of 4-wire E&M channel units.

5.03 Off-hook signal detection circuits supply the M-lead signal to the transmit converter for transmission to the far end. E-lead signals are relay controlled to provide either ground or battery-voltage levels (depending on strapping) for the received off-hook (busy) signal. On-hook signals output an E-lead open circuit. The E-lead relay is conditioned by a stored logic level in the receive-converter signaling register, which is updated every sixth received message-frame during normal operation. Refer to Table A for E&M lead conditioning during normal operation. During an alarm sequence, the signaling register is reset and the E-lead relay is conditioned by CGAC input from the alarm and power unit. Strapping options for E-lead conditioning and alarm sequencing are detailed in Table B of Section V of this manual.

5.04 All E&M channel units contain transmit and receive VF level adjustments, a BUSY switch, and a BUSY LED indicator. Actuation of the BUSY switch opens the TIP and RING interface (TIP 1 and RING 1 on four-wire units), and the E&M interface, which is opened toward the channel. The E-lead office interface is conditioned according to strapping. The BUSY indicator comes on to indicate channel active, or BUSY switch actuated.

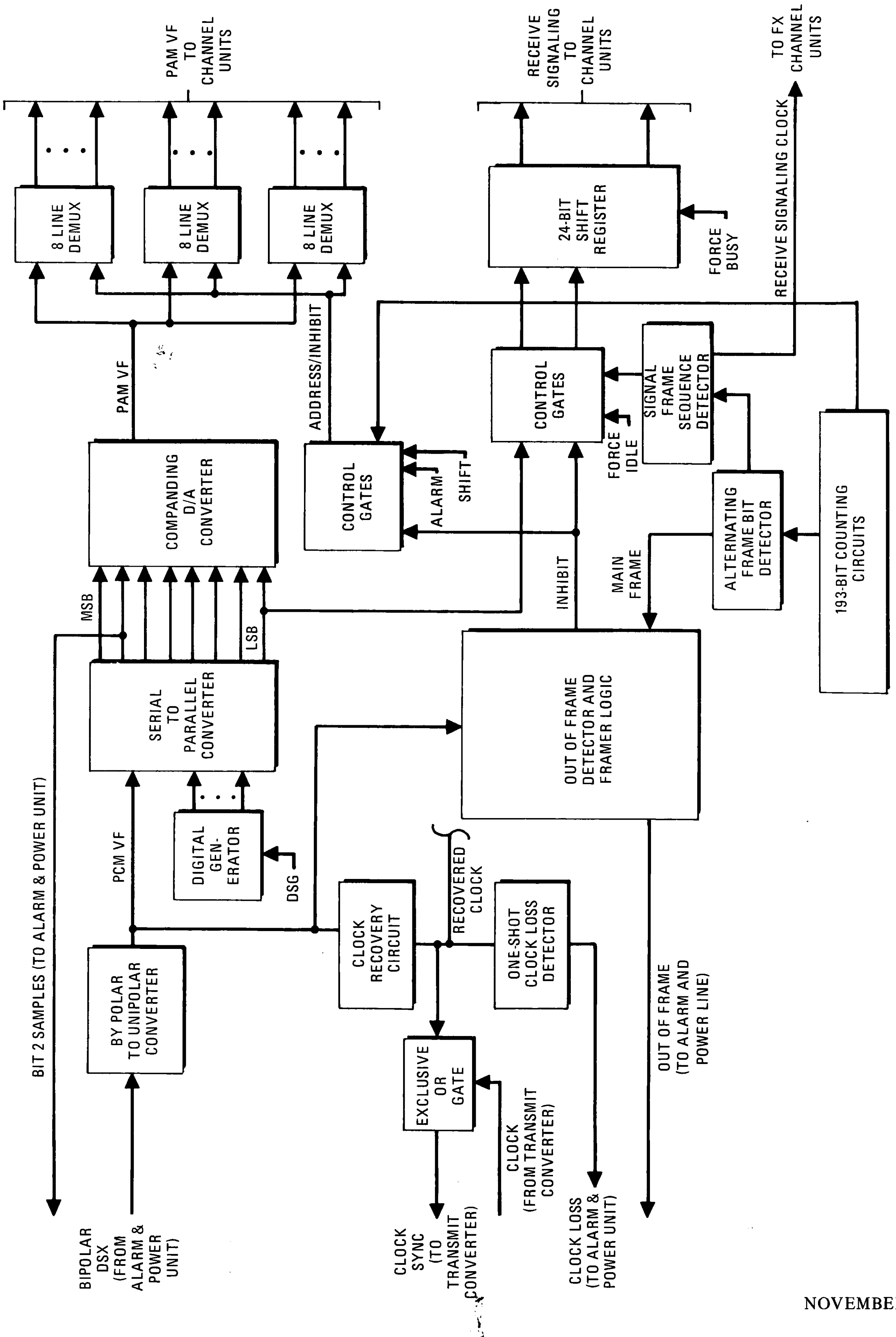

Fig. 6—Receive Converter Block Diagram

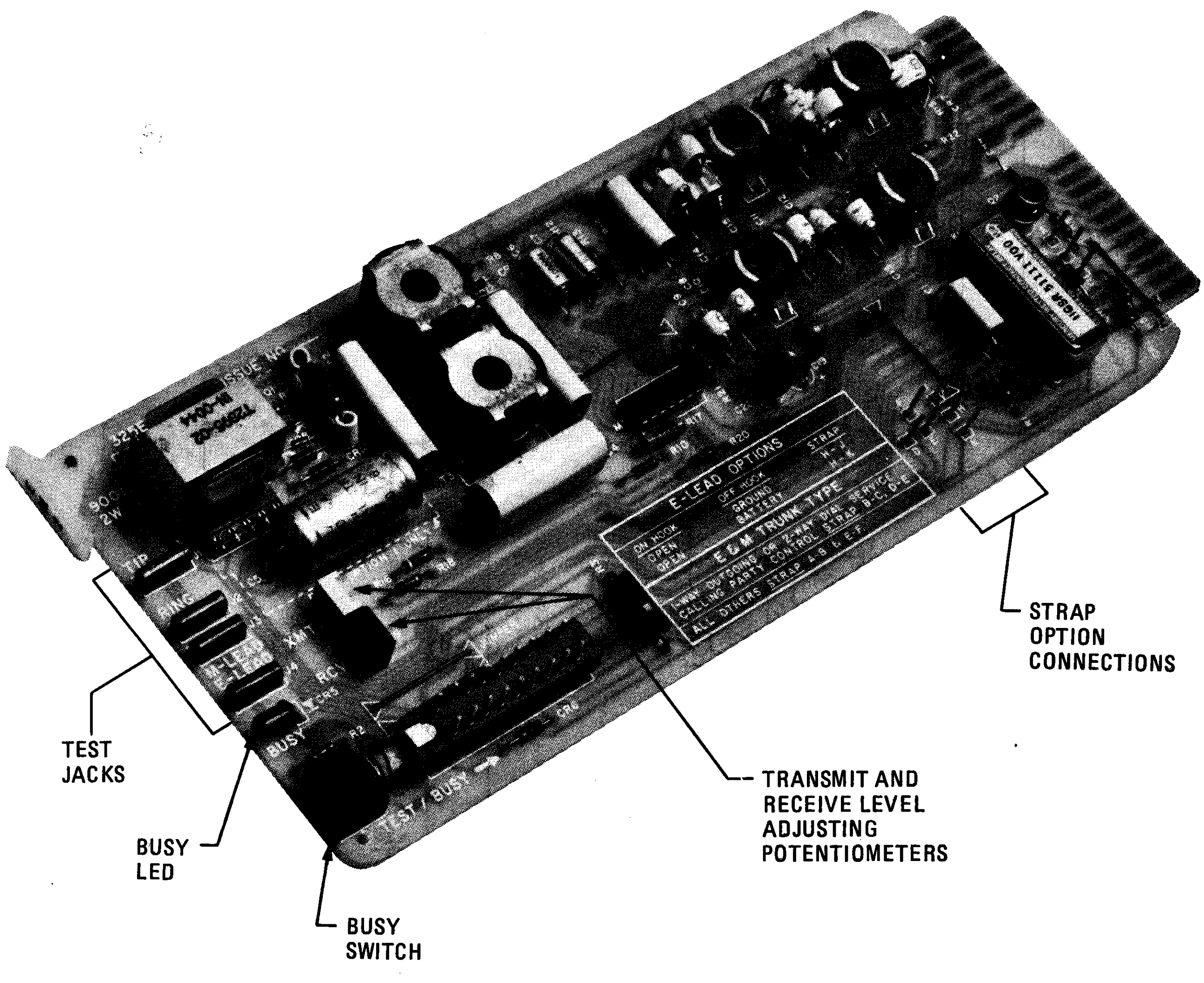

Fig. 7—Typical Channel Unit

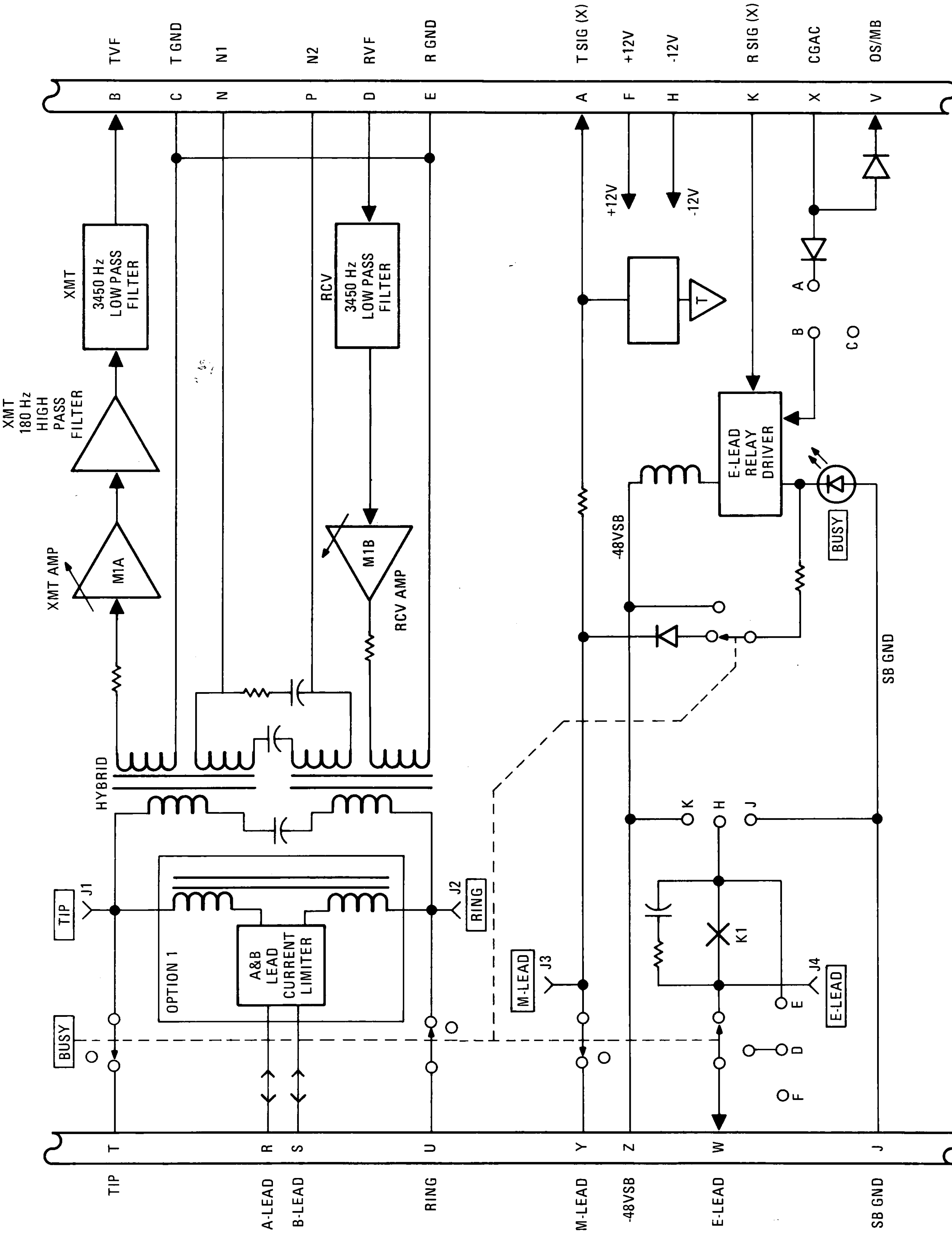

Fig. 8—E&M 2-Wire Channel Units (325EM02/03) Block Diagram

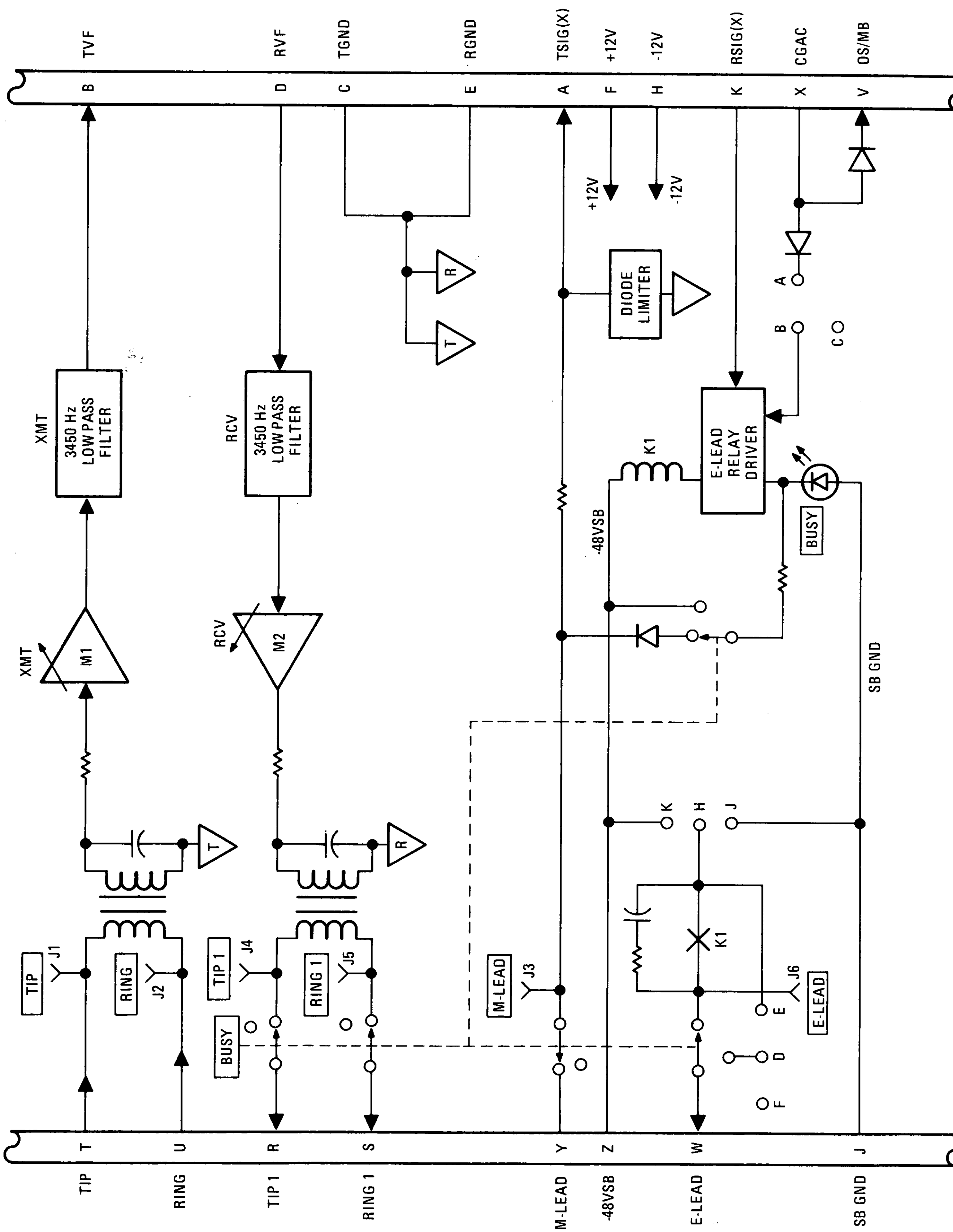

Fig. 9—E&M 4-Wire Channel Units (325EM01) Block Diagram

TABLE A

E&M LEAD SIGNAL CONDITIONING

E&M LEAD CONDITIONS FOR SIGNALING						
Originating Office				Terminating Office		
Calling Subscriber, Channel or Trunk State	E Lead	M Lead	Direction of Transmitted Signal	E Lead	M Lead	Called Subscriber State
Channel Idle	Open	Ground/Open	(none)	Open	Ground/Open	On-Hook
Channel Seized	Open	Battery	→	Ground or Battery	Ground/Open	On-Hook
Off-Hook (Conversation Period)	Ground or Battery	Battery	↔	Ground or Battery	Battery	Off-Hook

DIAL PULSE CHANNEL UNITS (325DP01, 325DP02)

5.05 Dial pulse channel units operate in tandem pairs with a dial pulse originating unit (325DP01) at the central office paired with a dial pulse terminating unit (325DP02) at the terminating office. Voice-frequency signals that enter the channel unit are amplified and then filtered by a 180-Hz to 3450-Hz bandpass filter before being applied to the transmit converter (325TC01). Trunk signaling (idle/busy) is level limited and also applied to the transmit converter.

5.06 Dial pulse originating units (Fig. 10) contain a tip-and-ring line reversal relay (K2) and a busy relay (K1). Relay K2 is controlled by receive signaling and also supplies an 800-ohm resistance battery (energized), or 800-ohm resistance ground (de-energized) output to the HS line. Relay K1 is controlled by a loop current detector and provides an open ATB lead output for busy conditions or a grounded ATB lead output for idle conditions. The S-lead output is also controlled through contacts of relay K1 and is strappable for a battery, or absence of ground (open) output, in the channel idle condition. In either case the line is grounded when the channel is busy. A solid-state switch is triggered by contacts of relay K1 to provide one ground pulse on the peg count line each time the channel becomes busy to toggle the office traffic counter. The solid-state (transistor) output is necessary to eliminate multiple counter pulsing, due to contact bounce across mechanical relay contacts. Actuation of the BUSY switch energizes relay K1 to busy the channel and open tip and ring during maintenance. A BUSY LED indicator reflects the state of relay K1.

5.07 CGA conditioning of the dial pulse originating unit is detailed in the following steps. Prior to an alarm condition, the CGAC input is a resistance battery connection and the CGAS input is a resistance ground connection. These levels allow normal operation of relays K1 and K2.

(a) Alarm detection causes the following conditions:

(1) CGAC input becomes 0 volts, which blocks all controls to relay K2 except for CGA commands during the total alarm sequence.

(2) CGAS input becomes a battery signal, which energizes relay K1 to busy the

TABLE B

FOREIGN EXCHANGE CHANNEL UNIT SIGNALING

TRANSMIT CONDITION	T-1 LINE SIGNALING D3 A	D3 B	D2 A	D2 B	RECEIVE CONDITION GROUND-START STRAPPING	RECEIVE CONDITION LOOP-START STRAPPING
325FX01 Channel Unit					325FX02 Channel Unit	
A. Loop open, no ring ground	0	1	0	0	A. Loop open (K1 out), no ring ground (K2 out)	A. Loop open (K1 out), no ring ground (K2 out)
B. Loop open, ring ground	0	0	0	1	B.1. (If transmitting tip ground) = loop open (K1 out), no ring ground (K2 out) B.2. (If not transmitting tip ground) = loop open (K1 out), ring ground (K2 in)	B. Loop open (K1 out), no ring ground (K2 out).
C. Loop closure, no ring ground	1	1	1	0	C. Loop closure (K1 in), no ring ground (K2 out)	C. Loop closure (K1 in), no ring ground (K2 out)
325FX02 Channel Unit					325FX01 Channel Unit	
A. No tip ground, no ringing	1	1	0	1	A. No tip ground (K1 out), no ringing (K2 out)	A. Tip ground (K1 in), no ringing (K2 out)
B. Tip ground, no ringing	0	1	1	1	B. Tip ground (K1 in), no ringing (K2 out)	B. Tip ground (K1 in), no ringing (K2 out)
C. Tip ground, ringing	0	0	1	0	C.1. (If transmitting loop closure) tip ground (K1 in), no ringing (K2 out) C.2. (If not transmitting loop closure) tip ground (K1 in), ringing (K2 in)	C.1. (If transmitting loop closure) tip ground (K1 in), no ringing (K2 out) C.2. (If not transmitting loop closure) tip ground (K1 in), ringing (K2 in)

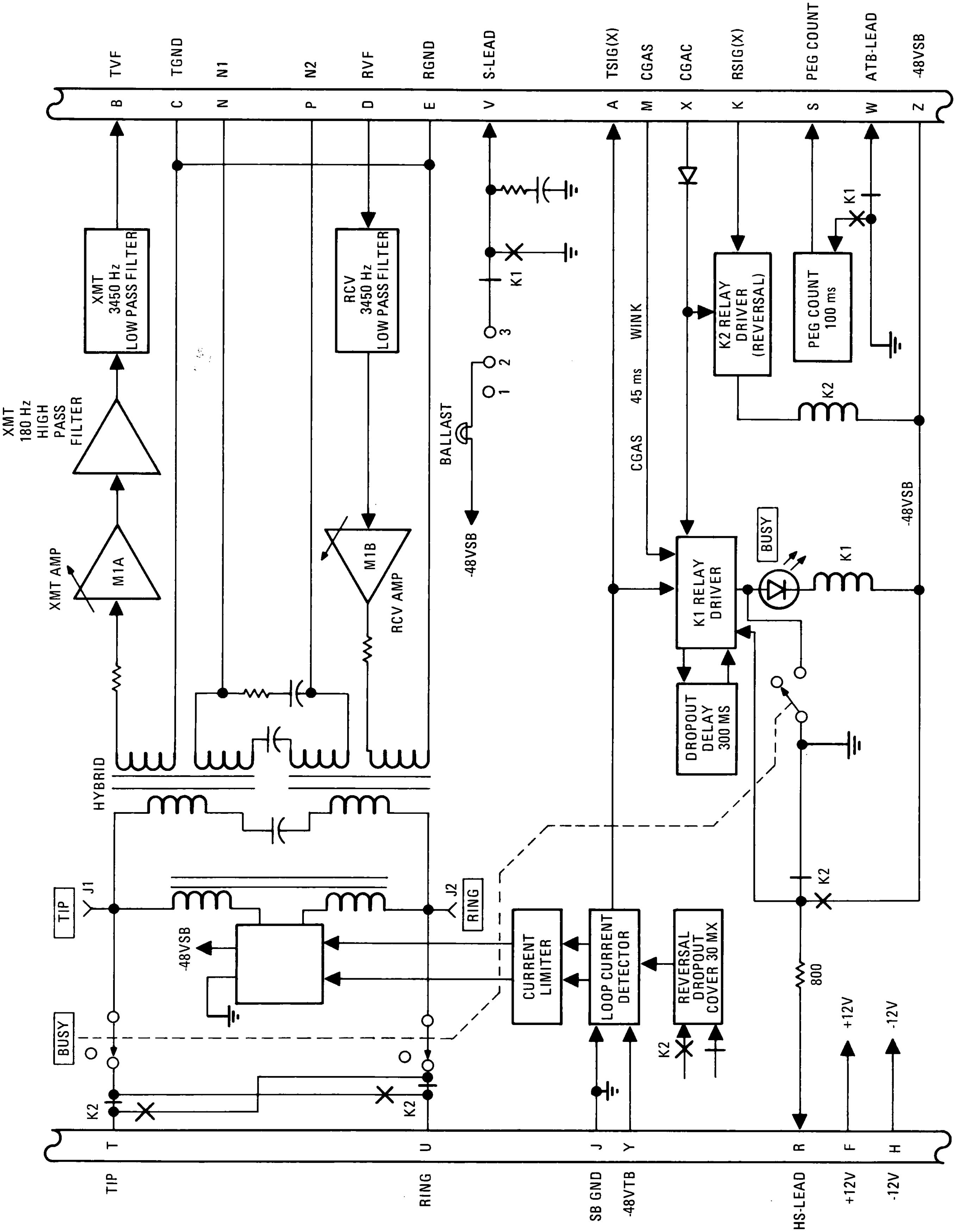

Fig. 10—Dial Pulse Originating Channel Units (325DP01) Block Diagram

channel. With relay K1 energized, the ATB lead output is an open circuit and the S-lead output is a ground connection.

(b) After approximately 12 seconds or 2 seconds (depending on alarm and power unit strapping), the CGAS input is pulsed to ground potential (winked). The wink signal momentarily de-energizes relay K1 and unbusies the channel to stop toll charges.

(c) This completes the first alarm sequence. Relay K1 will remain in the active state (BUSY) until cleared by the alarm and power unit trunk conditioning unit. The trunk conditioning unit requires a local alarm condition to be cleared for 12 seconds, before returning the CGAC and CGAS inputs to normal levels. For remote alarms, the CGAC and CGAS inputs are returned to normal levels as soon as the alarm clears.

5.08 Dial pulse terminating units (Fig. 11) contain a busy relay (K1), a BUSY switch, and a BUSY LED indicator. The busy relay provides line seizure and is controlled by receive signaling, CGA conditioning or the BUSY switch.

VOICE-FREQUENCY CHANNEL UNITS (325VF01)

5.09 See Fig. 12 for a block diagram of the VF channel unit. The 325VF01 channel unit provides four-wire VF transmit and receive paths only. There are no signaling provisions in this unit; therefore, external inband signaling must be provided if required. Input and output VF ports are balanced and provide 600-ohm impedances. An OS/MB-lead ground is provided during CGA.

FOREIGN EXCHANGE CHANNEL UNITS (325FX01, 325FX02)

5.10 See Fig. 13 for a block diagram of the 325-FX01 foreign exchange channel units and Fig. 14 for a block diagram of the 325FX02 channel units. The 325FX01 and 325FX02 foreign exchange channel units are functionally similar and are used as a complimentary pair in the B325 terminal system. Operated end-to-end, these units provide both a band-limited voice-frequency channel and the associated signaling for interfacing with PBX equipment in ground-start and loop-start modes. The 325FX01 (subscriber end) detects ring ground and loop closure and gives PBX ringing and loop current, while the 325FX02 (office end) detects tip ground and ringing and gives ring ground and loop closure to the central office.

5.11 The 325FX01 and 325FX02 channel units are both supplied with a three-position, toggle-type maintenance test switch (in addition to the BUSY switch), which may be used by the craftsman as an aid in isolating signaling malfunctions to a channel unit, common equipment unit or improper PBX/central office inputs. The switch is mounted towards the rear of the circuit board and is used with a channel unit extender (part of 325TK01 test kit) installed. The three switch positions, which are identified on the channel unit circuit board, are functionally explained below for each channel unit.

(a) 325FX01 (Subscriber)

(1) NORMAL (up) position: Completes circuit paths for normal control of relays K1 and K2 from receive converter signaling levels. Switch must remain in this position for normal channel operation.

(2) IDLE (center) position: Opens control circuit to relays K1 and K2 to inhibit tip ground and ringing.

(3) BUSY (down) position: Energizes relays K1 and K2 to apply tip ground and ringing to the subscriber. The subscriber should "ring trip" the unit when coming off-hook.

(b) 325FX02 (Office)

(1) NORMAL (up) position: Completes circuit paths for normal control of relays K1 and K2 from receive converter signaling. ***Switch must remain in this position for normal channel operation.***

(2) IDLE (center) position: Opens control circuit to relays K1 and K2 to inhibit ring ground and loop closure.

(3) BUSY (down) position: Energizes relays K1 and K2 to apply loop closure and ring ground (750 ohm) to the office.

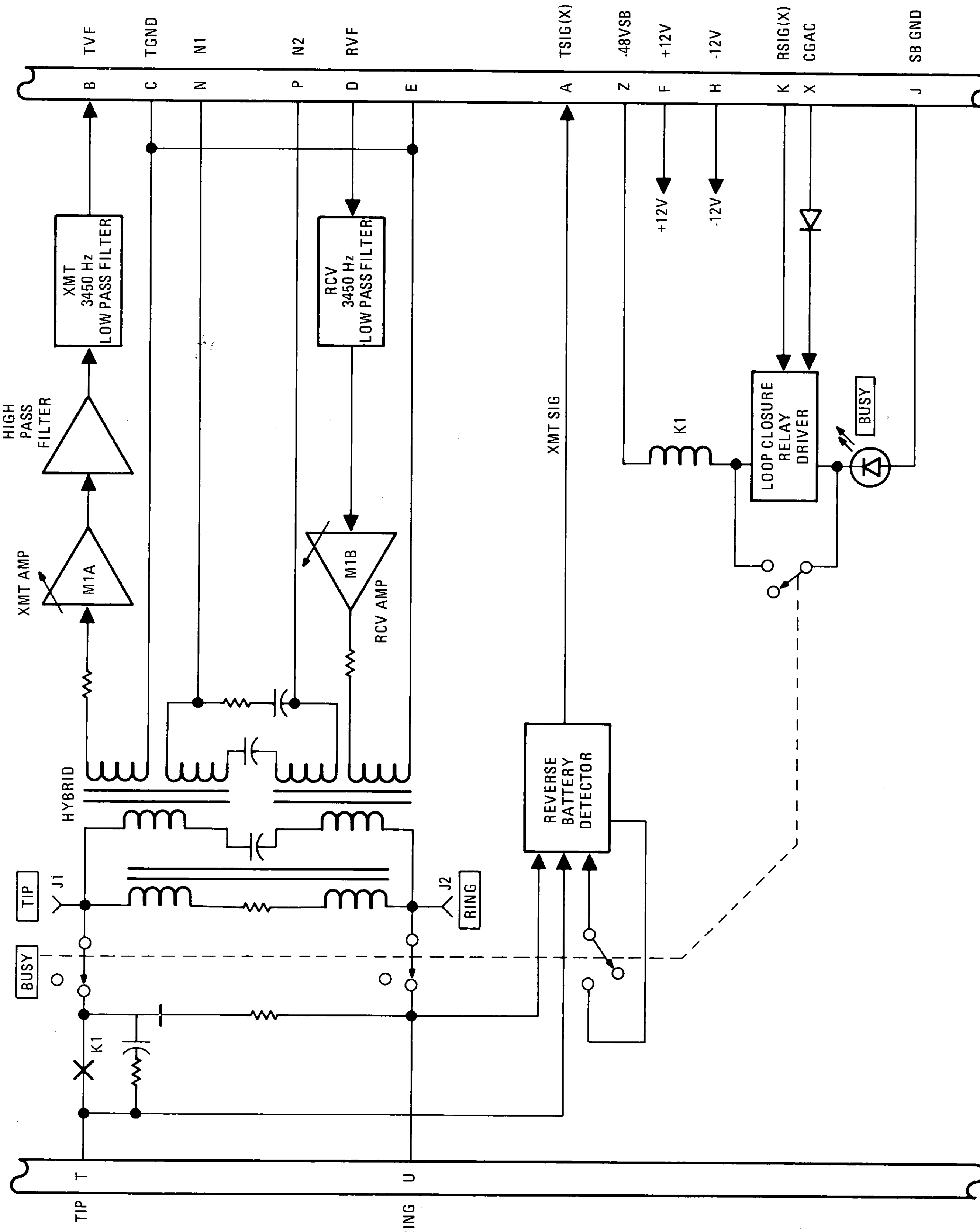

Fig. 11–Dial Pulse Terminating Channel Units (325DP02) Block Diagram

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Fig. 12—Voice-Frequency Channel Units (325VF01) Block Diagram

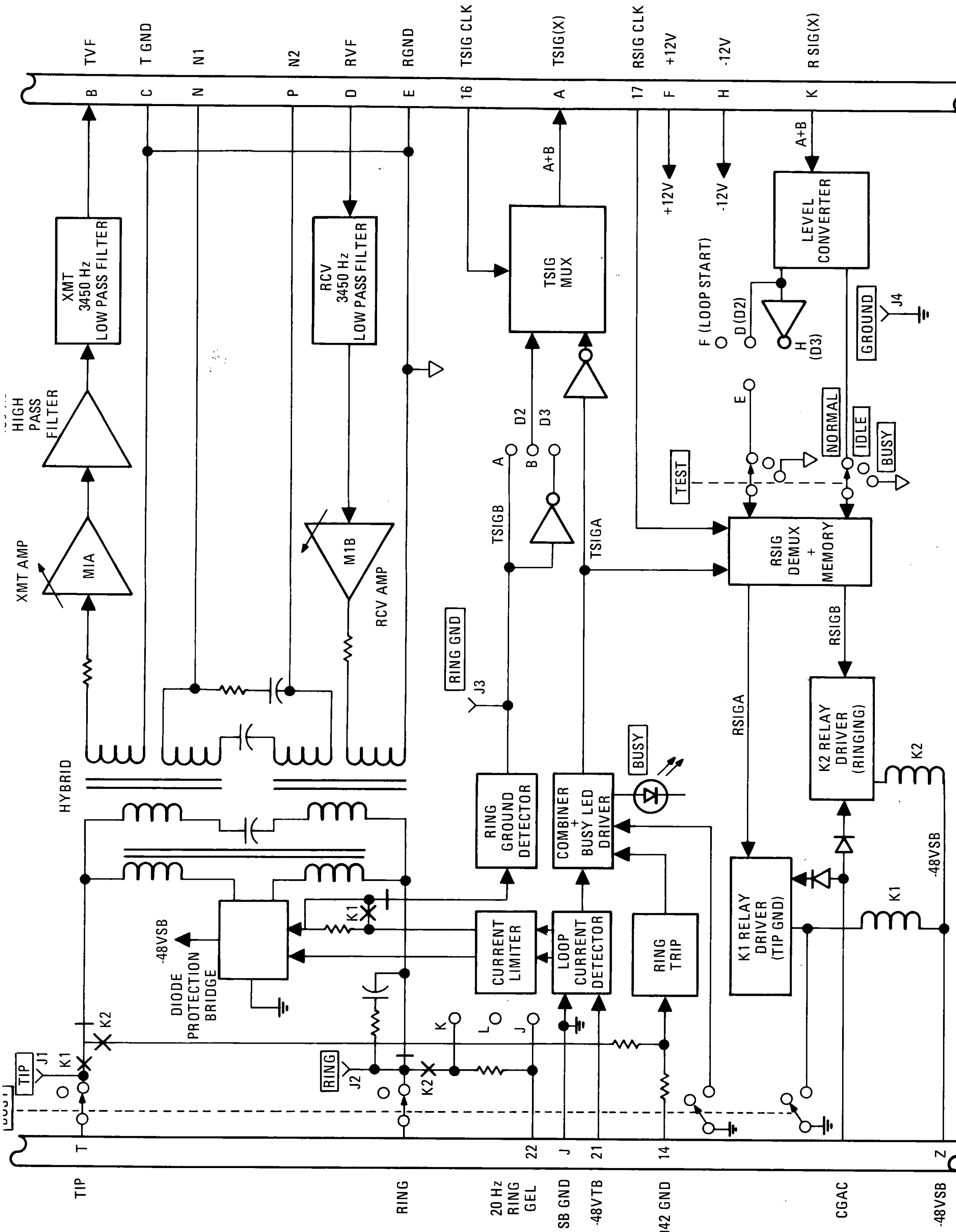

Fig. 13—Foreign Exchange Subscriber End Channel Units (325FX01) Block Diagram

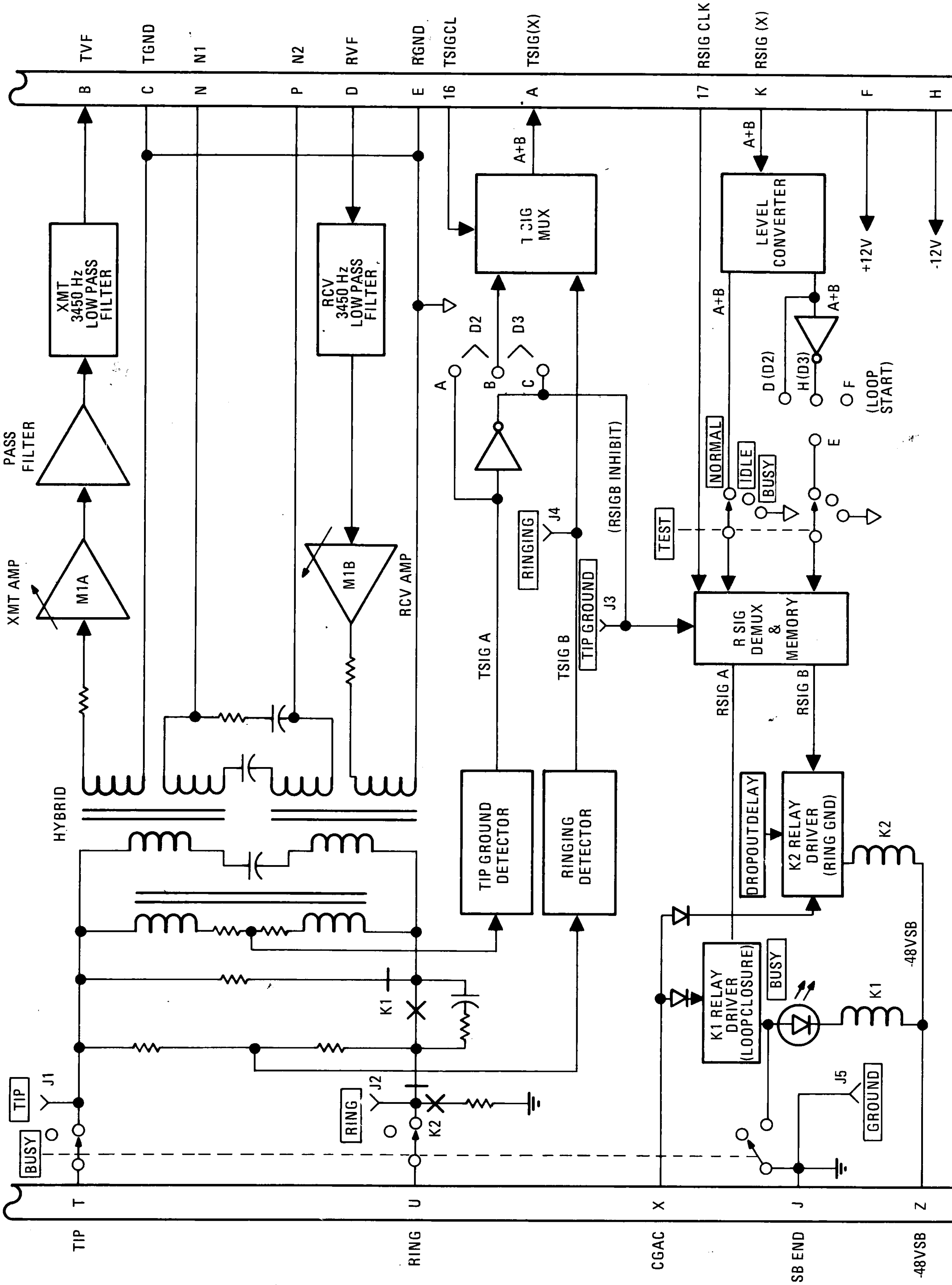

Fig. 14—Foreign Exchange Office End Channel Units (325FX02) Block Diagram

5.12 Strapping options are provided on both 325FX units to allow the user to configure for ground-start or loop-start operations. Table B defines loop-start and ground-start signaling conditions for the foreign exchange channel units.

6. TEST AND ALIGNMENT PANEL (325TA01)

6.01 The test and alignment panel block diagram is shown in Fig. 15. The panel provides necessary test jacks, switches, load circuits and filters to make channel gain adjustments and performance tests. Performance tests include idle channel noise, quantizing distortion, and interchannel crosstalk on a looped or end-to-end basis. A description of panel controls and test jacks is contained in Fig. 3, Section I, of this manual.

6.02 The test and alignment panel is constructed to two separate and isolated circuits. One circuit provides test oscillator connection to the transmit channel unit (XMT jack) through attenuation networks or straight wire connections and an impedance matching switch. The other circuit provides receive channel unit connection to the TEST OUT jack, with capability for inserting a distortion test filter or crosstalk test filter in the signal path. A receive channel unit impedance matching switch is also provided.

6.03 Facilities are provided for wiring an office milliwatt supply directly to the panel mating connector, thus eliminating the need for an externally-connected test oscillator. A gain adjustable amplifier may be strap-wired in series with the 1-kHz test input signal, if an office milliwatt input is used. Bypass straps eliminate the amplifier at installations where an external test oscillator is used.

7. D4 CONVERTER (To be supplied)

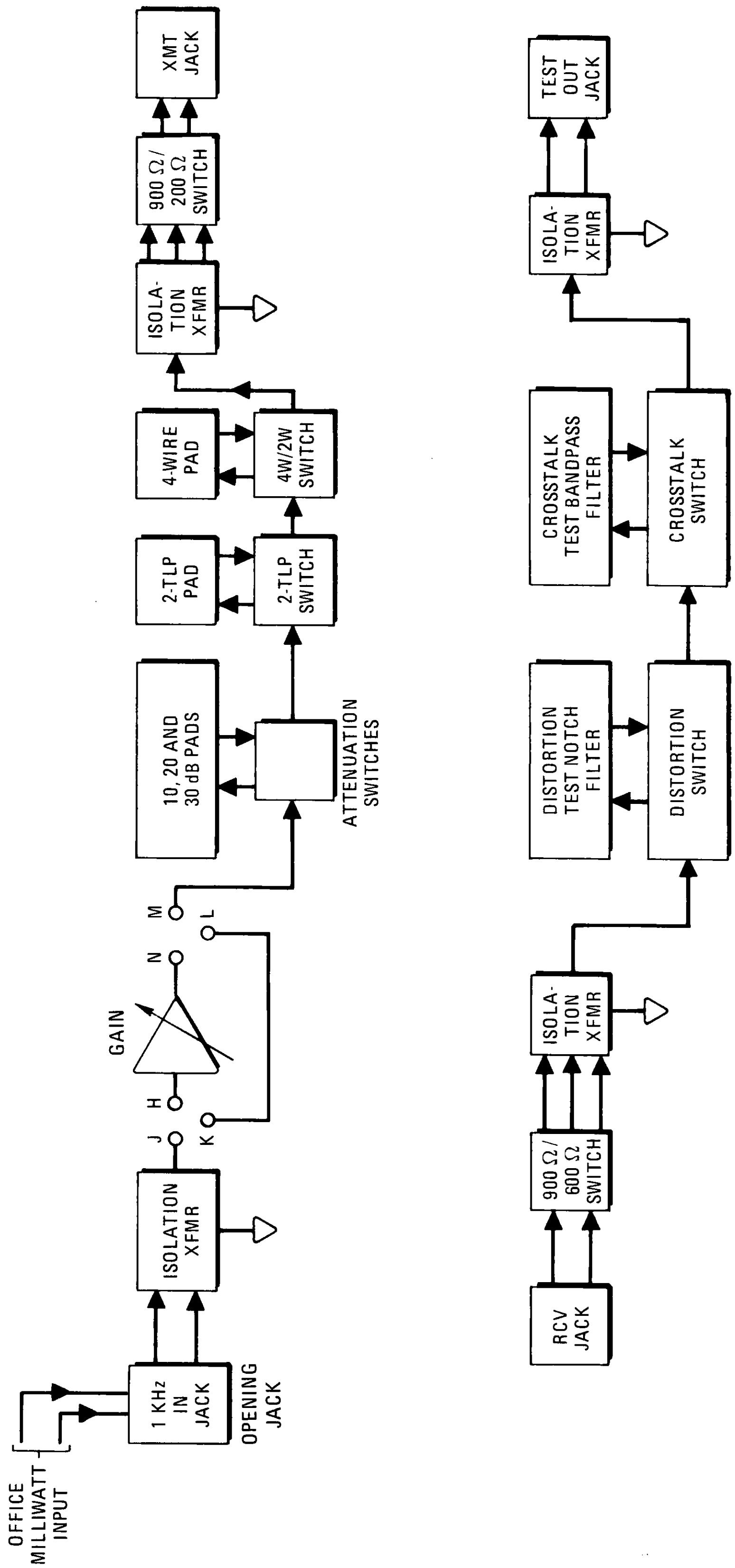

Fig. 15—Test and Alignment Panel Block Diagram

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Fig. 16—D4 Converter Block Diagram